CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI (C.G.)

M. TECH – Microelectronics and VLSI

Eligibility Criteria:

B.E./B.Tech. in ELX/ECE/ETC &EEE/E&I or M.Sc. Physics/Electronics with GATE qualifying marks in the Electronics / Electronics & Telecommunication Engineering.

SEMESTER I

S. No.	Board of Study	Subject Code	Subject	Periods per Week			Scheme of Examination Theory / Practical			Total Marks	Credit
				L	T	P	ESE	CT	TA		
1.	ET&T Engg.	588111(28)	MICROELECTRONICS TECHNOLOGY & IC FABRICATION	3	1	-	100	20	20	140	4
2.	ET&T Engg.	588112(28)	Basics of Micro-electronics & VLSI	3	1	-	100	20	20	140	4
3.	ET&T Engg.	572112(28)	Hardware Descriptive Languages	3	1	-	100	20	20	140	4
4.	ET&T Engg.	588113(28)	CMOS ANALOG INTEGRATED CIRCUITS	3	1	-	100	20	20	140	4
5.		**Elective – I**		3	1	-	100	20	20	140	4
6.	ET&T Engg.	588121(28)	Hardware Descriptive Languages Lab I	-	-	3	75	-	75	150	2
7.	ET&T Engg.	588122(28)	CMOS Integrated Circuits Lab II	-	-	3	75	-	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L- Lecture T- Tutorial

P- Practical, ESE- End Semester Exam

CT- Class Test, TA- Teacher's Assessment

Table-I

ELECTIVE – I

S. No.	Board of Study	Subject Code	Subject
1.	ET&T	588131(28)	Introduction to MEMS
2.	ET&T	588132(28)	MEMORY DESIGN AND TESTING
3.	ET&T	588133(28)	Optoelectronics
4.	ET&T	588134(28)	Microwave Integrated Circuits
5.	ET&T	588135(28)	Neural Networks for VLSI

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **MICROELECTRONICS TECHNOLOGY & IC FABRICATION** **Code: 588111(28)**
Total Theory Periods: **40 Codes**:
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I: Material properties:
crystal structure, lattice, basis, planes, directions, angle between different planes, characterization of material based on band diagram and bonding, conductivity, resistivity, sheet resistance, phase diagram and solid solubility, Crystal growth techniques, wafer cleaning, Epitaxy, Clean room and safety requirements.

Unit II Oxidation:
Kinetics of Silicon dioxide growth both for thick, thin and ultra thin films, thickness characterization methods, multi dimension oxidation modeling. Diffusion and Ion Implantation: Diffusion process, Solid state diffusion modeling, various doping techniques, Ion implantation, modeling of Ion implantation, statistics of ion implantation, damage annealing, thermal budget, rapid thermal annealing, spike anneal, advanced annealing methods Various deposition techniques CVD, PVD, evaporation, sputtering, spin coating .

Unit III: Etch and Cleaning:
materials used in cleaning, various cleaning methods, Wet etch, Dry etch, Plasma etching, RIE etching, etch selectivity/selective etch. Photolithography: Positive photo resist, negative photo resist, comparison of photo resists, components of a resist, light sources, exposure, Resolution, Depth of Focus, Numerical Aperture (NA), sensitivity, contrast, need for different light sources, masks, Contact, proximity and projection lithography, step and scan, optical proximity correction, develop(development of resist).

Unit IV :
Next generation technologies: Immersion lithography, Phase shift mask, EUV lithography, X-ray lithography, e-beam lithography, ion lithography, SCALPEL. Planarization Techniques: Need for planarization, Chemical Mechanical Polishing

Unit V :
Copper damascene process, Metal interconnects; Multi-level metallization schemes, Process integration: NMOS, CMOS and Bipolar process.

References:
1. James Plummer, M. Deal and P.Griffin, Silicon VLSI Technology, Prentice Hall Electronics
2. Stephen Campbell, The Science and Engineering of Microelectronics, Oxford University Press, 1996
3. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988
4. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983.
5. C.Y. Chang and S.M.Sze (Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Basics of Microelectronics & VLSI**
Total Theory Periods: **40** Code: **588112(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I: Introduction

MOSFET, threshold voltage, current, Channel length modulation, body bias effect and short channel effects, MOS switch, MOSFET capacitances, MOSFET models for calculation-Transistors and Layout, CMOS layout elements, parasitic, wires and vias-design rules-layout design SPICE simulation of MOSFET I-V characteristics and parameter extraction

Unit II: CMOS inverter:

static characteristics, noise margin, effect of process variation, supply scaling, dynamic characteristics, inverter design for a given VTC and speed, effect of input rise time and fall time, static and dynamic power dissipation, energy & power delay product, sizing chain of inverters, latch up effect-Simulation of static and dynamic characteristics, layout, post layout simulation

Unit III: Static CMOS design:

Complementary CMOS, static properties, propagation delay, Elmore delay model, power consumption, low power design techniques, logical effort for transistor sizing, ratioed logic, pseudo NMOS inverter, DCVSL, PTL, DPTL & Transmission gate logic, dynamic CMOS design, speed and power considerations, Domino logic and its derivatives, C2MOS, TSPC registers, NORA CMOS – Course project

Unit IV: Circuit design considerations of Arithmetic circuits

Arithmetic circuits, shifter, CMOS memory design - SRAM and DRAM, BiCMOS logic - static and dynamic behavior -Delay and power consumption in BiCMOS Logic

Unit V : VLSI Circuits and Systems

Introduction to VLSI systems; Timing circuit; Clock generators; Direct and PLL frequency synthesizer; Data converters; SAR, oversampled A/D and high speed converters; advanced A/D converters; filter design; Memory (volatile and non-volatile); DSP chip; CPU architecture; advanced low-power circuits.

References:

1. Sung-Mo Kang & Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis & Design, , MGH, Third Ed., 2003
2. Jan M Rabaey, Digital Integrated Circuits - A Design Perspective, Prentice Hall, Second Edition, 2005
3. David A. Hodges, Horace G. Jackson, and Resve A. Saleh, Analysis and Design of Digital Integrated Circuits, Third Edition, McGraw-Hill, 2004
4. R. J. Baker, H. W. Li, and D. E. Boyce, CMOS circuit design, layout, and simulation, Wiley-IEEE Press, 2007
5. Christopher Saint and Judy Saint, IC layout basics: A practical guide, McGraw-Hill Professional, 2001

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY

BHILAI (C.G.)

Semester: M. Tech. – I Branch: ET&T Engg.
Subject: **Hardware Descriptive Languages**
Total Theory Periods: 40 Codes: **572112(28)**
Total Marks in End Semester Examination: 100 TotalTutorial Periods: 12
Minimum No. of Class Tests to be Conducted: 02

UNIT- I Introduction to VHDL:-

Basic concepts of hardware description languages. Hierarchy, Concurrency, Logic and Delay modeling. Structural, Data-flow and Behavioral styles of hardware description.

UNIT- II Architecture of event driven simulators.

Syntax and Semantics of VHDL. Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations. Component instantiation .Concurrent and sequential constructs.Use of Procedures and functions, Examples of design using VHDL.

UNIT- III Model simulation:-

Simulation, Writing test bench, converting real and integer to time, Dumpingresult into text file, Reading vector from a text file, Test bench examples, Variable file names.

UNIT-IV Hardware modeling examples:-

Modeling entity interfaces, Modeling simple elements, Different types of modeling, Modeling regular structures, Modeling delays, Modeling conditional operations, Modeling synchronous logic, State machine Modeling, Interacting state machine, Modeling a Moore FSM, Modeling Mealy FSM, Generic priority encoder, Clock divider, Generic binary multiplier, Hierarchy in design.

UNIT- V Verilog:

Syntax and Semantics of Verilog.Variable types, arrays and tables. Operators, expressions and signal assignments. Modules, nets and registers, Concurrent and sequential constructs Tasks and functions, Examples of design using Verilog. Synthesis of logic from hardware description.

Texts:

1. J. Bhaskar, "VHDL Primer", Pearson Education Asia 2001.
2. J.Bhaskar, "Verilog HDL Synthesis - A Practical Primer", Star Galaxy Publishing,(Allentown, PA) 1998.
3. Douglas Perry, " VHDL programming by example" TMH 2004

References:

1. Z. Navabi, "VHDL", McGraw Hill International Ed. 1998.
2. S. Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Prentice Hall NJ, USA), 1996.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **ANALOG INTEGRATED CIRCUITS**
Total Theory Periods: **40** Code: **588114(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

UNIT I: SINGLE STAGE AMPLIFIERS

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT II: FREQUENCY RESPONSE AND NOISE ANALYSIS

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascade stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers. 7

UNIT III OPERATIONAL AMPLIFIERS

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION

General considerations, Multiple systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BIASING CIRCUITS

Basic current mirrors, cascade current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001.
3. Willey M.C. Sansen, "Analog design essentials", Springer, 2006.
4. Grebene, "Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, Douglas R.Holberg, "CMOS Analog Circuit Design", Second edition, Oxford University Press, 2002

ELECTIVE: I

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Introduction to MEMS**
Total Theory Periods: **40** Code: **588131(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I : Historical Background:
Silicon Pressure sensors, Micro-machining, Micro-Electro Mechanical Systems. Micro-fabrication and Micro-machining: Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA).

Unit II: Physical Micro-sensors :
Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors.

Unit III: **Micro-actuators** :
Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors-Micro-actuator systems

Unit IV:
Ink-Jet printer heads, Micro-mirror TV Projector. Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Poly-silicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials**.**

Unit V: Surface Micro-machined Systems :
Success Stories, Micro-motors, Gear trains, Mechanisms.; Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

Text/References

1. Stephen D. Senturia, "Micro-system Design" by, Kluwer Academic Publishers, 2001.
2. Marc Madou,
3. Fundamentals of Microfabrication by, CRC Press, 1997.Gregory Kovacs, Micromachined Transducers Sourcebook WCB McGraw-Hill, Boston, 1998.
4. M.-H. Bao, Micromechanical Transducers: Pressure sensors, accelrometers, and gyroscopes by Elsevier, New York, 2000.

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **MEMORY DESIGN AND TESTING**
Total Theory Periods: **40** Code: **588132(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I:

Random Access Memory Technologies Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Structures BiCMOS DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Unit II:

Nonvolatile Memories Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)- Bipolar PROMs-CMOS PROMs-Erasable (UV) Programmable Road-Only Memories (EPROMs)-Floating Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)- EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

Unit III:

Memory Fault Modeling, Testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Unit IV:

Semiconductor Memory Reliability And Radiation Effects General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

Unit V:

Advanced Memory Technologies and High-Density Memory Packaging Technologies Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories Magneto resistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

Text/References:

1. A.K Sharma, " Semiconductor Memories Technology, Testing and Reliability", IEEE Press.
2. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill.
3. Belty Prince, " Semiconductor Memory Design Handbook" • Memory Technology design and testing 1999 IEEE International Workshop on: IEEE Computer Society Sponsor (S)

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Opto Electronics**
Total Theory Periods: **40** Code: **588133(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

Unit I:
Nature of light, light sources, units of light, radio metric and photometric units, basic semi conductors, PN junction, carrier recombination and diffusion, injection efficiency, hetreo-junction, internal quantum efficiency, External quantum efficiency, double hetero junction, fabrication of heterojunction, quantum wells and super lattices.

Unit II:
Opto electronic devices, Optical modulators, modulation methods and modulators, transmitters, optical transmitter circuits, LED and laser drive circuits, LED-Power and efficiency, double hereostructure LED, LED structures, LED characteristics.

Unit III:
Laser modes, strip geometry, gain guided lasers, index guided lasers. Modulation of light, birefringence, electro optic effect, EO materials, Kerr modulators, scanning and switching, self electro optic devices, MO devices, AO devices, AO modulators.

Unit IV:
Display devices, Photoluminescence, cathode luminescence, EL display, LED display, drive circuitry, plasma panel display, liquid crystals, properties, LCD displays, numeric displays.

Unit V:
Photo detectors, thermal detectors, photoconductors, detectors, photon devices, PMT, photodiodes, photo transistors, noise characteristics of photo-detectors, PIN diode, APD characteristics, APD Design of detector arrays, CCD, Solar cells.

Text/References:

1. Opto electronics - An introduction - J Wilson and J F B J iS Hawkers. (Prentics-Hall India, 1996)
2. Optical fibre communication - J M Senior (Prentice Hall India (1985)
3. Optical fibre communication systems - J Gowar (Prentice Hall 1995).
4. Introduction to optical electronics - J Palais (Prentice Hall, 1988)
5. Semiconductor opto electronics - Jasprit Singh (McGraw-Hill, Inc, 1995)
6. Semiconductor optoelectronic devices - P Bhattacharya (Prentice Hall of India, 1995)
7. Fibre Optics and Opto-electronics, R P Khare (Oxford University Press, 2004)

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: Microwave Integrated Circuits
Total Theory Periods: **40** Code: **588134(28)**
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be Conducted: **02**

Unit I:
Introduction to microwave integrated circuits: Active and passive components.
Unit II:
Analysis of micro strip lines: variational method, conformal transformation, numerical analysis; losses inmicrostrip lines; Slot line and Coupled lines;
Unit III:
Design of power dividers and combiners, directional couplers, hybrid couplers, filters.
Unit IV:
Microstrip lines on ferrite and garnet substrates; Isolators and circulators;
Unit V:
Lumped elements in MICs. Technology of MICs: Monolithic and hybrid substrates; thin and thick filmtechnologies, computer aided design.

Textbooks/References:

1. Leo Young and H. Sobol, Ed. Advances in Microwaves, Vol.2, Academic Press Inc., 1974.
2. B.Bhat and S. Koul, Stripline-like transmission lines for MICs, John Wiley, 1989.
3. T.K. Ishii, Handbook of Microwave Technology

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY
BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Neural Networks for VLSI**
Total Theory Periods: **40** Code: 588232(28)
Total Marks in End Semester Examination: **100** Total Tutorial Periods: **12**
Minimum No. of Class Tests to be conducted: **02**

UNIT I

Introduction: History, overview of biological Neuro-System, Mathematical Models of Neurons

UNIT II

ANN architecture, Learning rules, Learning Paradigms-Supervised, Unsupervised and reinforcement Learning.

UNIT III

Supervised Learning and Neuro-dynamics: Perceptron training rules, Delta, Back propagation training algorithm, Hopfield Networks, Associative Memories.

UNIT IV

Unsupervised and Hybrid Learning: Principal Component Analysis, Self-organizing Feature Maps, ARTnetworks, LVQ

UNIT V

Applications for VLSI Design: Applications of Artificial Neural Networks to Function Approximation, Regression, Classification, Blind Source Separation, Time Series and Forecasting.

Text:

1. Anderson J.A., "An Introduction to Neural Networks", PHI, 1999
2. Haykin S., "Neural Networks-A Comprehensive Foundations", Prentice-Hall International, New Jersey, 1999.

Reference:

1. Freeman J.A., D.M. Skapura, "Neural Networks: Algorithms, Applications and Programming Techniques",Addison-Wesley, Reading, Mass, (1992).
2. Golden R.M., "Mathematical Methods for Neural Network Analysis and Design", MIT Press, Cambridge,MA, 1996.
3. Cherkassky V., F. Kulier, "Learning from Data-Concepts, Theory and Methods", John Wiley, New York,1998.

LABS

CHHATISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY BHILAI (C.G.)

Semester: **M. Tech. – I** Branch: ET&T Engg.
Subject: **Hardware Descriptive Language Lab I**
Total Lab Periods: 40 Code: 588121(28)
Total Marks in End Semester Examination: **75**

Lab Experiments

1. Write a VHDL & Verilog Program to implement a 3:8 decoder,16:1 MUX
2. Write a VHDL & Verilog Program to implement 4 bit addition/subtraction
3. Write a VHDL& Verilog Program to implement a.4 bit comparator
4. Write a VHDL & Verilog Program to implement a Mod- 10 up counter
5. Write a VHDL & Verilog Program to perform serial to parallel transfer of 4 bit binary number
6. Write a VHDL & Verilog Program to design a 2 bit ALU containing 4 arithmetic & 4 Logic operations
7. Write a VHDL & Verilog Program to generate the 1010 sequence detector. The overlapping patterns are allowed.
8. Write a VHDL & Verilog Program to generate the 1010 sequence detector. The overlapping patterns are notallowed
9. Experiment on VHDL& Verilog program to design 4 bit shift register.
10. Experiment on VHDL& Verilog program to design Tflip flop & JK FlipFlop(toggle).
11. Experiment on VHDL& Verilog program to design JK flip flop.
12. Experiment on VHDL & Verilog program to design asynchronous binary up counter.
13. Experiment on VHDL & Verilog program to design BCD up - down counter.
14. Design Melay machine using VHDL.& Verilog
15. Design Moore machine using VHDL.& Verilog

BHILAI (C.G.)

Semester: M. Tech. – I **Branch: ET&T Engg.**

Subject: CMOS Integrated Circuits Lab II

Total Lab Periods: 40 **Code: 588122(28)**

Total Marks in End Semester Examination: 75

Lab Experiments

Schematic capture, circuit simulation, layout design, DRC, layout extraction and post-layout simulation, parasitic extraction and GDS II of following circuits

1. CMOS Inverter.
2. CMOS NAND gate
3. CMOS NOR gate
4. Resistance for a specific value.
5. Capacitor for a specific value.
6. JK Flip Flop
7. Differential amplifier
8. Current Mirror
9. 4:1 MUX
10. Op-Amp