RCET, BHILAI

Chhattisgarh Swami Vivekanand Technical University Bhilai

Scheme of teaching and examination

M.Tech. (DIGITAL ELECTRONICS) in the Department of Electronics & Telecommunication

II Semester

S.No	Board of Study	Subject Code	Subject Name	Periods per week			Scheme of Exam			Total Marks	Credit L+(T+P)/2
				L	T	P	Theory/Practical				
							ESE	CT	TA		
1	Electronics & Telecom.	555211 (28)	Digital System Design using VHDL	3	1	-	100	20	20	140	4
2	Electronics & Telecom.	555212 (28)	Electronics System Design	3	1	-	100	20	20	140	4
3	Electronics & Telecom.	555213 (28)	Microcontroller & Embedded System	3	1	-	100	20	20	140	4
4	Electronics & Telecom.	555214 (28)	Computer Communication Network	3	1	-	100	20	20	140	4
5	Refer Table - II		Elective –II	3	1	-	100	20	20	140	4
6	Electronics & Telecom.	555221 (28)	Digital System Design using VHDL Lab	--	-	3	75	--	75	150	2
7	Electronics & Telecom.	555222 (28)	Electronics System Design Lab	-	-	3	75	--	75	150	2
Total				**15**	**5**	**6**	**650**	**100**	**250**	**1000**	**24**

L-Lecture, T- Tutorial, P- Practical, ESE- End Semester Examination, CT- Class Test, TA- Teacher's Assessment
Note : Duration of all theory papers will be of Three Hours.

Table – II		
Elective – II		
Board of Study	**Code**	**Subject**
Electronics & Telecom.	555231 (28)	Artificial Intelligence & Expert System
Electronics & Telecom.	555232 (28)	Advanced Satellite Communication
Electronics & Telecom.	555233 (28)	Cellular Network Design
Electronics & Telecom.	555234 (28)	Digital Image Processing

Note (1) – **1/4th of total strength of students subject to minimum of twenty students is required to offer an elective in the college in a Particular academic session .**

Note (2) – **Choice of elective course once made for an examination cannot be changed in future examinations.**

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.** Branch: **Electronics & Telecom**
Subject: **Digital System Design using VHDL** Code: **555211 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: 02

UNIT - I
Introduction to VHDL, design units, data objects, signal drivers. inertial and transport delays. delta delay, VHDL data types, concurrent and sequential statements.

UNIT - II
Subprograms -Functions. Procedures, attributes, generic, generate. Package. IEEE std logic library, file I/o, test bench, component declaration, instantiation, configuration

UNIT - III
Combinational logic circuit design and VHDL implementation of following circuits - fast adder, subtractor, decoder, encoder, multiplexer. ALU, barrel shifter, 4X4 key hoard encoder, multiplier, divider, Hamming code encoder and çorrection circuits.

UNIT - IV
Synchronous sequential circuit design — *finite* state machines, Mealy and Moore, UNIT- UNIT- state assignments. design and VHDL implementation of FSMs, Linear feedback, shift register(pseudo random and CRC)

UNIT - V
Asynchronous sequential circuit design — primitive flow table, concept of race, critical race arid hazards. design issues like metastability. synchronizers. clock skew and timing considerations .Introduction to place & route process ,introduction to ROM, PLA, PAL, architecture of CPLD(Xilinx/ altera), FPGA architecture(Xilinx/ altera)

Text Books:

1. VHDL 3rd Edition, Douglas Perry, McGraw-Hill
2. J. Bhaskar, “ A VHDL Primer”, Addison Wesley, 1999.

Reference Books:

1. M. Ercegovac, T. Lang and L.J. Moreno, ”Introduction to Digital Systems”, Wiley,2000
2. C. H. Roth, “Digital System Design using VHDL”, PWS Publishing
3. J.F. Wakerly, “Digital Design-Principles and Practices”, Prentice Hall International
4. Michae John Sebastian Smith, “Application-Specific Integrated Circuits”, Addison Wesley.
5. Z. Navabi, “ VHDL-Analysis and Modeling of Digital Systems”, MGH

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.** Branch: **Electronics & Telecom**
Subject: **Electronics System Design** Code: **555212 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I

Methods of solution of network, Network equations and formulations, DC , AC and transient analysis of networks, Simulation examples using Spice or other relevant packages.

UNIT – II

Types of modeling , Models of diode, BJT and FET, Design and simulation of Logic circuits and analog circuits, Sensitivity and optimization of networks and functions.

UNIT – III

Features, levels of abstraction, elements, simulation process, types of simulators, FSM modeling, test benches, generics & attributes, synthesis tools features & optimization in VHDL, Synthesis guidelines, Timing issues : terminology, flow diagram, clock, gated clock, setup & hold time, violation, metastability, static & dynamic timing analysis.

UNIT – IV

CMOS & Bi-CMOS logic families & PLD architecture, Power dissipation, noise and ESD issues, clock distribution, signal connections, synchronous and asynchronous design features, and memory system design. Classification of CPLD architecture, CPLD 9500 series, Xilinx FPGA –XC4000 series, designing steps in ASIC.

UNIT – V

Logic Simulation: Problems in simulation based design verification, Type of simulation, The unknown logic value, compiled simulation, Event-driven simulation, Delay models, Elements evaluation, Haazard detection, Gate level event driven simulation, Transition-Independent nominal transport delays simulation engines**.**

Text Books:

1. Computer methods for circuit Analysis and Design – L. Vlach & K. Singhal
2. Computer Aided Analysis and Design of Electronic Circuits – Grimblay J.B.
3. Digital systems testing and testable design by M.Abramovici, M.A. Breuer, A.D. Friedman; Jaico Publishing House

Reference Books:

1. James E. Buchanan Bicmos – CMOS System design – McGraw Hill
2. VHDL - Douglas Perry, McGraw Hill Publication
3. Using Testbenches- Janic Bergerson
4. VHDL Modeling for Digital Design Synthesis.- Yu. Chin Hsu, K. Tsai Kluwer publishers.
5. Xilinx PLD data manual

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.**
Branch: **Electronics & Telecom**
Subject: **Microcontroller & Embedded System Design**
Code: **555213 (28)**
Total Theory Periods: **40**
Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I
Overview of Embedded System:- Embedded System, Categories of Embedded System, Requirements of Embedded Systems, Challenges and Issues in Embedded Software Development, Applications of Embedded Systems in Consumer Electronics, Control System, Biomedical Systems, Handheld computers, Communication devices.

UNIT – II
Embedded Hardware & Software Development Environment :- Hardware Architecture, Micro- Controller Architecture, Communication Interface Standards, Embedded System Development Process, Embedded Operating systems, Types of Embedded Operating systems.

UNIT – III
8 Bit microcontrollers Architecture on chip peripherals instruction set/programming of Intel MCS51 family (8 bit) microcontroller, Interfacing of 8051 with LCD, ADC, sensors, stepper motor, key board, DAC, Memory interfacing.

UNIT – IV
Real Time & Database Applications :- Real- Time Embedded Software Development, Sending a Message over a Serial Link, Simulation of a Process Control System, Controlling an Appliance from the RTLinux System, Embedded Database Applications using examples like Salary Survey, Energy Meter Readings.

UNIT – V
Microchip PIC16 family PIC16F873 processor features architecture memory organization register file map I/O ports PORTA - PORTB PORTC Data EEPROM and flash program memory Asynchronous serial port SPI mode I2C mode.

Text Books:

1. Programming for Embedded Systems- Dreamtech Software Team, Wiley Dreamtech
2. The 8051 micro controllers , M A Mazidi& Mazidi, Pearson Education
3. Design with PIC micro-controllers: John B Peatman, Pearson Education

Reference books:

1. Fundamentals of Embedded Software where C and Assembly Meet Daniel W Lewis.
2. DS101374: National Semiconductor reference manual.
3. Embedded / Real Time systems: Concepts, Design and programming, Dreamtech Software Team, Jhon Wiley & Sons.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.**
Branch: **Electronics & Telecom**
Subject: **Computer Communication Network**
Code: **555214 (28)**
Total Theory Periods: **40**
Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I
Review of computer networking concepts: Topology, LAN, WAN, MAN, Internet, OSI/ISO, TCP/IP reference models, Point to point protocols. **ARQ:** Retransmission strategies.

UNIT – II
Functional elements : Multiplexing, Switching , Networks Management & traffic controls. Delay models in Data Networks Switching techniques: Performance measures & architectural issues.

UNIT - III
Internetworking: TCP/IP Internet architecture, IPV4, IPV6, IP addressing & related issues, IP address resolution techniques (ARP). IP datagram & forwarding, routing algorithms.

UNIT – IV
Multiple access techniques: ALOHA, CSMA, CSMA/CD, CSMA/CA, CDMA, OFDM, Delay throughput characteristics, WLAN-Protocols, multiple access, Ad-hoc networks, Bluetooth Specifications, WAP.

UNIT – V
Network security issues: Ciphers, DES, Public key cryptography, RAS algorithm, Digital Watermarking, Attacks and Counter Measures , Service Authentication Proforma.

Text Books:

- Tananbaum A.S., “Computer Networks”, 3rd Ed, PHI, 1999.
- Stallings W., “Computer Communication Networks”, PHI.

Reference Books:

- Black U., “Computer Networks-Protocols, Standards and Interfaces”, PHI, 1996.
- Stallings W., “SNMP, SNMPv2, SNMPv3, RMON 1&2”, 3rd Ed., Addison Wesley, 1999.
- Michael A. Miller, “Data & Network Communications”, Vikas Publication.
- William A. Shay, “Understanding Data Communications & Networks”, Vikas Publication.
- Data Networks, Dimitri Bertisekas & Robert Gallager, PHI
- Local Area Networks”, Gerd E Kieser – Mc-Graw-Hill
- Computer Networks and Internetworking” D.E.Comer, Pearson Education
- Cryptography and Network Security: Principles and Practice”,William Stallings, Pearson Education
- GSM, CDMA and 3G Systems” , Steele,, Wiely Students Edition
- Communication Networking” An analytical approach” Anurag kumar, D. Manjunath & Joy Kuri– Morgn – Kaufmann publishers

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.**
Branch: **Electronics & Telecom**
Subject: **Artificial Intelligence & Expert System**
Code: **555231 (28)**
Total Theory Periods: **40**
Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT – I
Scope of AI: Games, theorem proving, natural language processing, vision and speech processing, robotics, expert systems, AI techniques- search knowledge, abstraction.

UNIT – II
Problem solving: State space search; Production systems, search space control: depth-first, breadth-first search, heuristic search - Hill climbing, best-first search, branch and bound. Problem Reduction, Constraint Satisfaction End, Means-End Analysis

UNIT – III
Knowledge Representation: Predicate Logic: Unification, modus ponens, resolution, dependency directed backtracking. Rule based Systems : Forward reasoning: conflict resolution, backward reasoning: use of no backtrack.
Structured Knowledge Representation: Semantic Nets: slots, exceptions and default frames, conceptual dependency, scripts.

UNIT – IV
Handling uncertainty: Non-Monotonic Reasoning, Probabilistic reasoning, use of certainty factors, fuzzy logic.

UNIT – V
Learning: Concept of learning, learning automation, genetic algorithm, learning by inductions, neural nets.
Expert Systems: Need and justification for expert systems, knowledge acquisition, Case studies: MYCIN, RI.

Text Books:

- E. Rich and K. Knight, “Artificial intelligence”, TMH, 2nd ed., 1992.
- N.J. Nilsson, “Principles of AI”, Narosa Publ. House, 1990.

Reference Books:

- D.W. Patterson, “Introduction to AI and Expert Systems”, PHI, 1992.
- Peter Jackson, “Introduction to Expert Systems”, AWP, M.A., 1992.
- R.J. Schalkoff, “Artificial Intelligence - an Engineering Approach”, McGraw Hill Int. Ed., Singapore, 1992.
- M. Sasikumar, S. Ramani, “Rule Based Expert Systems”, Narosa Publishing House, 1994.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.**
Branch: **Electronics & Telecom**
Subject: **Advanced Satellite Communication**
Code: **555232 (28)**
Total Theory Periods: **40**
Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT - I
Orbital Mechanics: Orbit Equations, Orbit Description, Locating the Satellite in the Orbit and with Respect to Earth, Orbital Elements. Look Angle Determination and Visibility. Orbital Perturbations, Orbit Determination, Launch Vehicles, Orbital Effects in Communication Sys. Performance.

UNIT – II
Spacecraft: Communication Subsystems, Transponders, Antennas, Equipment Reliability.
Earth Stations. The Space Link, Satellite Link Design. Basic Transmission Theory. System Noise Temp., G/T Ratio, Noise Figure, Downlink Design, Design of Satellite Links for Specified C/N.

UNIT - III
Multiple Access. FDMA, FDM/FM/FDMA. Calculating the Overall Carrier to Noise Ratio on a FDM/FM/FDMA Link. Backoff. Measuring & Calculating the Effects of Intermodulation Noise. Overdeviation and Companding. Companded Single Side Band. Preassigned and Demand Assignned FDMA.

UNIT – IV
Time Division Multiple Access. Frame Structure and Design. Reference Burst, Preamble, Network Synchronization, Unique Word Detection. TDMA. Channel Capacity, Preassigned and Demand Assignned TDMA, Speech Interpolation and Prediction, Downlink Analysis for Digital Transmission.

UNIT – V
Satellite Services: Satellite mobile communication, VSAT technology, Direct Broadcast by satellite (DBS).Global Positioning System. Radarsat.

Text books:

1. T. Pratt and C. W. Bostian. *Satellite Communications*, John Wiley & Sons, 1986.
2. R. M. Gagliardi, *Satellite Communications*, Lifetime Learning Publications, Belmont, CA, 1984.

Reference Books:

1. W.L. Pritchard, H. G. Suyderhoud, and R. A. Nelson, *Satellite Communication System Engineering*, 2nd Ed., Prentice Hall, 1993.
2. J.J. Spilker , Digital Communication by satellite , PH Publication
3. J. Martin, Communication satellite systems, PH publication

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.** Branch: **Electronics & Telecom**
Subject: **Cellular Network Design** Code: **555233 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT- I
The Cellular Concept: evolution of mobile radio communication. Cellular telephone system, frequency reuse, channel assignment and handoff strategies. Interference and system capacity, trunking and grade of service, improving capacity in cellular system.

UNIT- II
The mobile radio environment: -BPSK, QPSK transmission and detection techniques, pi/4-QPSK transmission and detection techniques, QAM, GMSK.
Multiple access techniques: Introduction to multiple accesses, FDMA, TDMA, Spread spectrum multiple access, Frequency hopped multiple access (FHMA). Code division multiple access (CDMA), Space division multiple access (SDMA)

UNIT- III
The mobile radio environment: causes of propagation path loss, causes of fading, long term and short term, definition of sample average. Statistical average. Probability density function, cumulative probability distribution, level crossing rate and average duration of fade, delay spread, coherence bandwidth, intersymbol interference

UNIT- IV
Equalization, diversity and channel coding: fundamentals of equalization, space polarization, frequency and time diversity, polarization diversity, frequency and time diversity, fundamentals of channel coding.

UNIT- V
GSM-Global System for Mobile: services and features, GSM system architecture, GSM radio subsystem. GSM channel types, GSM frame structure, signal processing in GSM,introduction to CDMA, digital cellular standard.

Text Books:
- Wireless Communication: Principles and Practice by T.S. Rappaport. Prentice Hall International
- Mobile communication-Design fundamentals by William C.Y. Lee, John Wiley.

Reference Books:

- Raj Pandya, “Mobile and Personal Communication systems and services”, Prentice Hall of India, 2001.
- Theodore S.Rappaport, “Wireless communications:Principles and practice”, third Indian reprint Pearson Education Asia 2003.
- C.Y.William Lee, “Mobile cellular telecommunications”, 2nd edition Mc.Graw Hill Inc.1995.
- Jochen Schiller, “Mobile communications”, fifth Indian reprint, Pearson Education Ltd. 2000.
- Yi-Bing Lin and Imrich Chlamtac, “Wireless and Mobile Network Architectures”' 2001, John Wiley &Sons.
- Garg.V.K “IS-95 CDMA and CDMA 2000”, first Indian reprint 2002, Pearson Education ltd.
- Stallings.W “Wireless communications and networks”, second Indian reprint 2002, Pearson Education Ltd.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, Bhilai

Semester: **M.E. II Sem.** Branch: **Electronics & Telecom**
Subject: **Digital Image Processing** Code: **555234 (28)**
Total Theory Periods: **40** Total Tut Periods: **12**
Total Marks in end Semester Exam.: **100**
Minimum number of class tests to be conducted: **02**

UNIT - I
Digital image representation, elements of digital processing systems, sampling and quantization, simple image model, basic relationship between pixel and image geometry

UNIT - II
Image transforms, introduction to Fourier transform, DFT, properties of 2D DFT, FFT, other separable image transform, DCT, DST, Walsh, Harr transforms

UNIT - III
Image enhancement: basic gray level transformation, histogram processing using arithmetic and logical operations, spatial filtering, smoothening and sharpening filters , smoothing and sharpening frequency domain filters.

UNIT - IV
Image compression-fundamentals, image compression models, information theory, free compression, lossy compression, image compression standards

UNIT - V
Image segmentation- detection of discontinuities, edge lending and boundary detection, region based segmentation. Representation and description: representation, boundary descriptor, and regional descriptor.

Text:

1. Rafael C. Conzalez & Richard E. Woods, “Digital Image Processing”, AWL.
2. A.K. Jain, “Fundamental of Digital Image Processing”, PHI.

Reference:

1. Rosefield Kak, Digital Picture Processing,
2. Digital Image Processing, W. K. Pratt.(3 Ed.) John.Wiley.
3. Digital Image Processing & Computer vision : An introduction to theory & Implementation” by Robert Jschalkoff – John wiley & Sons Inc.
4. Digital Image Processing, K. R. Castleman, PHI
5. Digital Image Processing & Analysis, B. Chanda and D.Mujumdar, PHI, New Delhi, 2000.

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: **M.E. I Sem.** Branch: **Electronics & Telecom.**
Subject: **Digital System Design using VHDL Lab** Code: **555221 (28)**
Total Practical Periods: **40** Total Tut Periods: **Nil**
Total Marks in end Semester Exam.: **75**

List of Experiment to be performed

1) To design and simulate the basic gates
2) Designing of the combinational blocks
   a) Mux b) Encoders c) Decoders
3) Designing and simulation of Code converters
4) Designing, simulation and implementation 9-bit parity generator/checker
5) Designing, simulation and implementation Flip-Flops
6) Designing and simulation of Registers
7) Designing and simulation of Counters
8) FSM modeling (Design Sequence Detector “101”)
9) Designing, simulation and implementation of ROM
10) Designing, simulation and implementation of RAM
11) Designing, simulation and implementation of FIFO
12) Design, simulation and implementation of ALU
13) Designing and simulation of Filter
14) Designing and simulation of FSK modulator and Demodulator
15) Designing and simulation of PN generator.

List of Equipments/Machine/Software etc. Required :

1) Computer System with Pentium IV Processor, 256MB RAM
2) EDA tools:
   i. FPGA implementation kit
   ii. CPLD implementation kit
   iii. Xilinx project nevigator 5.2
   iv. Active HDL 6.2
   v. Modelsim

Recommended Books:

1) Fundamentals of Digital Logic with VHDL Design: Brown Vranesic, TMH Publication.
2) VHDL Primer Bhaskar PHI Publication

CHHATTISGARH SWAMI VIVEKANAND TECHNICAL UNIVERSITY, BHILAI

Semester: **M.E. I Sem.**
Subject: **Electronics System Design Lab**
Total Practical Periods: **40**
Total Marks in end Semester Exam.: **75**

Branch: **Electronics & Telecom.**
Code: **555222 (28)**
Total Tut Periods: **Nil**

List of Experiments:

- Three experiments on Design of diode based circuits
- Three experiments on Simulation of diode based circuits
- Three experiments on Design of transistor based circuits
- Three experiments on Simulation of transistor based circuits
- Three experiments on Design of OPAMP based circuits
- Three experiments on Simulation of OPAMP based circuits

List of Equipments/Machines/Software etc.:
MATLAB with Simulink, SPICE, Discrete components for the design of the circuits, Function generator, CRO, Power Supply, PCB Work station etc.

Reference Books:
CAD of Electronic Circuits by B. Raghuram, PHI.