PANJAB UNIVERSITY, CHANDIGARH-160014 (INDIA)

(Estd.under the Panjab University Act VII of 1947-enacted by the Govt. of India)

FACULTY OF ENGINEERING & TECHNOLOGY

SYLLABI

AND THE

REGULATIONS

FOR

M.Tech. (Microelectronics)
2018-19

SCHEME OF EXAMINATION FOR
MASTER OF TECHNOLOGY (MICROELECTRONICS)
Scheme of Examination 2018-19

FIRST SEMESTER

S.No	Course Code	Course Name	Scheme of Teaching			Scheme of Examination			
			L-T-P	Contact hrs/week	Credits	Theory			Practical*
						Internal Assessment	University Assessment	Total	
1	MIC 101	Semiconductor Device physics	3-0-2	5	4	50	50	100	50
2	MIC 102	Integrated Circuit Technology.	3-0-2	5	4	50	50	100	50
3	MIC 103	MOS Integrated Circuit Modeling.	3-0-2	5	4	50	50	100	50
4	MIC 104	HDL and VLSI Design.	3-0-2	5	4	50	50	100	50
5		Elective- I	3-0-2	5	4	50	50	100	50
6	MIC 108	Research Seminar- I	0-0-3	3	1	----	----	----	50
Total			**15-0-13**	**28**	**21**	**250**	**250**	**500**	**300**

***** Practical marks are for continuous and end semester evaluation

Total Marks: 800 **Total Credits: 21**

Elective-I

MIC 105 Computer Aided Design Methodologies and Tools.
MIC 106 Material Science & Engineering.
MIC 107 Embedded System Design.

SECOND SEMESTER:

S.No	Course Code	Course Name	Scheme of Teaching			Scheme of Examination			
			L-T-P	Contact hrs/week	Credits	Theory			Practical*
						Internal Assessment	University Assessment	Total	
1	MIC 201	Measurement and Characterization Techniques.	3-0-2	5	4	50	50	100	50
2	MIC 202	Architecture of VLSI System.	3-0-2	5	4	50	50	100	50
3	MIC 203	Analog and Mixed Signal Device Design.	3-0-2	5	4	50	50	100	50
4	MIC 204	Advanced Memory Technology and Design.	3-0-2	5	4	50	50	100	50
5		Elective- II	3-0-2	3	4	50	50	100	50
6	MIC 208	Research Seminar-II	0-0-3	3	1	----	----	----	50
Total			**15-0-13**	**26**	**21**	**250**	**250**	**500**	**300**

***** Practical marks are for continuous and end semester evaluation

Total Marks: 800 **Total Credits: 21**

Elective- II

MIC 205 Digital Integrated Circuits and Systems.
MIC 206 MEMS and Microsystems.
MIC 207 RF and High Speed Digital Design.

THIRD SEMESTER

S.No	Course Code	Course Name	Scheme of Teaching			Scheme of Examination			
			L-T-P	Contact hrs/week	Credits	Theory			Practical*
						Internal Assessment	University Assessment	Total	
1	MIC 301	Low Power Digital CMOS Design	3-0-2	5	4	50	50	100	50
2		Elective- III	3-0-2	5	4	50	50	100	50
3	MIC 304	Preliminary Thesis	0-0-20	20	10	----	----	---	100
Total			**6-0-24**	**30**	**18**	**100**	**100**	**200**	**200**

***** Practical marks are for continuous and end semester evaluation

Total Marks: 400 **Total Credits = 18**

Elective- III

MIC 302 Microelectronic Packaging and Testing

MIC 303 Nano Scale Devices and Systems

FOURTH SEMESTER:

S.No	Course Code	Course Name	Scheme of Teaching			Scheme of Examination		
			L-T-P	Contact hrs/week	Credits	Practical Marks		
						Internal Assessment	University Assessment	Total
1	MIC 401	Thesis	0-0-30	30	15	100	100	200
Total			**0-0-30**	**30**	**15**	**100**	**100**	**200**

***** Practical marks are for continuous and end semester evaluation

Total marks: 200 **Credits = 15**

Internal Assessment of Thesis (ECE 7201) will be graded as follows:

S. No.	Grade	Requirement
1.	**A+**	Publication from Thesis in SCI/SCIE indexed Journal
2.	**A**	Publication from Thesis in Scopus/ESCI indexed Journal
3.	**B+**	Publication from Thesis in Proceedings of International/ National Conference

Total M.TECH. Marks: 2200 **Total M.E. Credits: 75**

FIRST SEMESTER

Course Code	**MIC-101**
Course Title	**SEMICONDUCTOR DEVICE PHYSICS**
Type of Course	Core
L T P	3 0 2
Credits	4
Course Assessment Methods End Semester Assessment (University Exam.) Continuous Assessment (Sessional, Assignments, Quiz)	 50 50

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION-A

Properties of Semiconductor Physics: Energy Bands in Metals, Semiconductors, and Insulators, Direct and Indirect Semiconductors, Variation of Energy Bands with Alloy Composition, Electrons and Holes, Effective Mass, charge carriers in semiconductor, Extrinsic and intrinsic semiconductor, Electrons and Holes in Quantum Wells, Carrier Concentration, (6)

Carrier Transport Phenomena: Carrier Drift ,Carrier Diffusion ,Graded Impurity Distribution, The Hall Effect, Semiconductor equations and carrier statistics: Poisson's and continuity equations; Introduction to quantum theory of solids: Fermi-Dirac statistics and Boltzmann approximation to the Fermi-Dirac statistics; Semiconductor Diodes; (6)

Non-equilibrium Excess Carriers in Semiconductors: Carrier Generation and recombination, Characteristics of Excess Carriers, Ambipolar Transport ,Quasi-Fermi Energy Levels, Excess-Carrier Lifetime ,Surface Effects. (6)

The p-n Junction: Base structure of the p-n Junction, p-n Junction current, Barrier formation in metal-semiconductor junctions, Semiconductor model, Generation and Recombination currents, Junction break down, charge storage and transients. (5)

SECTION-B

Semiconductor Hetero- junctions: CV characteristics and dopant profiling, IV characteristics, Small signal models of diodes . Energy band diagrams. (4)

Bipolar Transistors : BJT action, minority carrier distribution, low frequency CB current gain, equilibrium circuit Models. (6)

Junction Field Effect Transistor: JFET concepts, device characteristics, non-ideal effects, equivalent circuit and frequency limitation. (6)

Metal Oxide Semiconductor Field Effect Transistors: Metal semiconductor ohmic contacts, MOS structure and operation , capacitance -voltage characteristics ,small signal equivalent circuits, non-ideal effects. (6)

TEXT BOOKS			
S. No.	Title	Author(s)	Publisher
1	Solid State Electronic Devices	G. Streetman, and S. K. Banerjee	7th edition, Pearson
2	Semiconductor Physics and Devices	Neamen , D. Biswas	McGraw-Hill Education
RECOMMENDED BOOKS			
1	Physics of Semiconductor Devices	S. M. Sze and K. N. Kwok	3rd edition, John Wiley &Sons
2	Fundamentals of solid state electronics	C.T. Sah	World Scientific Publishing Co. Inc

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-102**
Course Title	**INTEGRATED CIRCUIT TECHNOLOGY**
Type of Course	Core
L T P	3 0 2
Credits	4
Course Assessment Methods End Semester Assessment (University Exam.) Continuous Assessment (Sessional, Assignments, Quiz)	 50 50

SYLLABUS

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SECTION-A

Goals of semiconductor manufacturing: Cost, Quality, Variability, Yield, Reliability. Monolithic IC Processes: Silicon Wafer preparation, wafer cleaning techniques, defects, clean room concept, Unit processes: diffusion systems, Ion implantation, thermal oxidation, photolithography, fine-line lithography, etching, Epitaxy, Chemical Vapour Deposition(CVD) techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films, Metallization, Crystal growth and wafer preparation. (12)

Mask generation, Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects, Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques, RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits, Advanced MOS technologies, IC Packaging: IC Packaging: Die Separation, Package Types, Attachment Method. (10)

SECTION-B

Monolithic Components: Bipolar IC process, p-n junction isolation, monolithic bipolar transistor construction, dielectric isolation; MOS device fabrication techniques; CMOS FET technologies: SOS CMOS Process, Twin well CMOS Process, Problems in CMOS process. (12)

Process modeling**:** Regression Modeling, Single-Parameter Model, Two-Parameter Model, Residuals, Standard Error, Analysis of Variance, Precision of Estimates, Linear Model with Nonzero Intercept, Multivariate Models, Nonlinear Regression, Regression Chart. (11)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1.	VLSI Technology	S. M. Sze	McGraw Hill
2.	Silicon VLSI Technology	James D. Plummer and Micheal D. Deal	Pearson Education
RECOMMENDED BOOKS			
1.	Fundamentals of Semiconductor Fabrication	Gary S.May, S.M.Sze	Wiley Publications
2.	Fundamentals of Semiconductor Manufacturing and Process Control	Gary S. May, Costas J. Spanos	A JOHN WILEY & SONS, INC., PUBLICATION
3.	Semiconductor Material and device characterization	Dieter K. Schroder	Wiley Publications
4.	ULSI Technology	C.Y. Chang and S.M. Sze	McGraw Hill Companies Inc, 1996

Practical:

1. Introduction to process simulation tools, e.g. SUPREM, MINIMOS, STEPS etc.
2. Simulation of typical MOS processes and MOSFET Characteristics, extraction of parameters for circuit simulation.

Course Code	**MIC-103**
Course Title	**MOS INTEGRATED CIRCUIT MODELLING**
Type of Course	Core
L T P	3 0 2
Credits	4
Course Assessment Methods End Semester Assessment (University Exam.) Continuous Assessment (Sessional, Assignments, Quiz)	 50 50

SYLLABUS

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SECTION-A

MOS Transistor : The Metal oxide Semiconductor Structure, The MOS system under external Bias, Structure and Operation of MOS Transistor, MOSFET current-voltage Characteristics, MOSFET Scaling and Small-Geometry effects, MOSFET, level 1 Model Equation and parameters. (10)

MOS Inverter Static Characteristics: Introduction, Resistive-Load Inverter, Inverter with n-Type MOSFET Load, CMOS Inverter. (6)

CMOS Inverter Switching Characteristics: Introduction, Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints. (6)

SECTION-B

Combinational MOS Logic Circuits: Introduction, MOS Logic Circuits with Depletion nMOS Loads, CMOS Logic Circuits, Complex Circuits, CMOS Transmission Gates (Pass Gates), BiCMOS logic. (8)

Sequential MOS Logic Circuits: Introduction, Behavior of Bistable Elements, SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, CMOS D-Latch and Edge-Triggered Flip-Flop. (6)

Dynamic Logic Circuits: Introduction, Basic Principles of Pass Transistor Circuits, Voltage Bootstrapping, Synchronous Dynamic CMOS Circuit Techniques, High-Performance Dynamic CMOS Circuits. (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1.	CMOS Digital Integrated Circuit Analysis and Design	Sung-Mo Kang and Yusuf Leblebici	TATA McGraw Hill
RECOMMENDED BOOKS			
1	Introduction to VLSI Systems	Mead and Convey	Addison Wesley. 1982
2	VLSI Design Techniques for Analog and Digital Circuits	Randall Geiger	McGraw Hill.2000
3	Operation and Modeling of the MOS Transistor	Yannis Tsividis	McGraw Hill International Edition, 1999
4	Digital Integrated Circuits	Jan M. Rabaey	Prentice Hall of India, (New Delhi), 1997.

PRACTICALS

- Simulation using schematic editor
- Schematic page editor. Part editor, programmer's editor,
- Session Log editing properties- spreadsheet editor property editor.
- Hierarchical design- Hierarchical blocks, ports, pins
- Placing, editing and connecting parts
- Editing and adding graphics
- Configuring a macro
- Creating a netlist
- Exporting and importing schematic data
- Editing and creating models
- Simulation Parameters
- D.C Sweep Analysis, Transient Analysis, Parametric Analysis and Performance Analysis

Course Code	**MIC-104**
Course Title	**COMPUTER AIDED DESIGN METHODOLOGIES AND TOOLS**
Type of Course	Core
L T P	3 0 2
Credits	4
Course Assessment Methods End Semester Assessment (University Exam.) Continuous Assessment (Sessional, Assignments, Quiz)	 50 50

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION-A

Introduction to VLSI design methodologies and supporting CAD tool environment. Overview of C and Data structures, Graphics and CIF, concepts and structure and algorithms for some of the CAD tools. (9)

Introduction to Unix/Linux, Introduction to SPICE application of SPICE for analog design, writing netlist design and circuit simulation using NGSPICE, Introduction to Layout Tool and IC Layout Design,, Introduction to Physical Verification (LVS, DRC and PEX) Post Layout Simulation with circuit example. (12)

SECTION-B

Schematic editors, layout editors, Module generators, silicon compliers, placement and routing tools. (12)

Behavioral, functional, logic and circuit simulators, Aids for test vector generation and testing. Introduction to Verilog/VHDL languages, behavior level, gate level and dataflow Modeling; RTL coding, logic synthesis and static timing analysis. Design Verification using Test benches. FPGA Design Flow Altera Quartus II . (12)

(*Project using CAD tools*)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Computer Aids for VLSI	Steven M. Rubin	Addison-Wesley, 1980
RECOMMENDED BOOKS			
1	Algorithms for VLSI Design Automation	Sabin H.Gerez	John Wiley. 2000
2	An introduction to VLSI Physical design	Majid Serafzadeh	McGraw Hill.2002
3	Application specific integrated circuits	Michael John Sabastian	Smith Pearson Education (LPE).2001Edition, 1999

PRACTICAL

Study of

- schematic,
- layout editors,
- layout of gates, cells,
- layout optimization,
- use of silicon compliers.

Course Code	**MIC-105**
Course Title	**HDL AND VLSI DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Introduction To Hardware Design : Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction. (5)

VHDL Background : VHDL History, Existing Languages, VHDL Requirements, The VHDL Language. (5)

Design Methodology Based on VHDL : Elements of VHDL, - Data objects- Variable signal, and constant, Data types, Operators and signal assignments, Design Suits- Entities, architecture declaration, configurations, Packages, Top down Design, Top down Design with VHDL, Subprograms, VHDL Operators, Conventions and Syntax. (8)
Basic Concepts In VHDL : Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments. (4)

SECTION-B

Design Organization : Definition and Usage of Subprograms, Packaging Parts and Utilities, Generic and configuration, Design Configuration and Libraries. (6)

Utilities For High-Level Descriptions : Type Declarations , VHDL Operators, Subprogram Parameter Types and Overloading, Predefined Attributes, User Defined Attributes. (6)

Behavioral Description of Hardware : Process Statement, Assertion Statement, Sequential Wait Statements. (5)

Verilog: Overview of Digital design with Verilog HDL, basic concepts, modules & ports. (6)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	VHDL	Douglas Perry	Tata Mc Graw Hill 2004
RECOMMENDED BOOKS			
1	VHDL Analysis & Modelling of Digital system	Navabi Z	McGraw Hill.2002
2	VHDL for Designers	sjoholm and Lindh	Prentice Hall International,1998
3	Digital system Design using VHDL	Roth. C.H.	Thomson learning,2000

PRACTICALS:

Practical based on theory will be conducted on VHDL

Course Code	**MIC-106**
Course Title	**MATERIAL SCIENCE & ENGINEERING**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Material Science: Introduction, processing & selecting materials, looking at Materials by Powers of Ten. Atomic Bonding**:** Atomic Structure, The Ionic Bond, The Covalent Bond, The Metallic Bond, The Secondary or van der Waals, Bond Materials-The Bonding Classification. (6)

Crystalline Structure & Defects: Metal Structures, Ceramic Structures, Polymeric Structures, Semiconductor Structures, Lattice Positions, Directions, and Planes. Point Defects, Linear Defects, Planar Defects-Two Dimensional Imperfections Non-crystalline Solids- Three Dimensional Imperfections. Thermal Production of Point Defects, Solid State Diffusion, Steady- State Diffusion, Alternate Diffusion Paths (8)

Mechanical and Thermal Behavior: Mechanical: Stress versus Strain, Elastic Deformation, Plastic Deformation, Hardness, Creep and Stress Relaxation, Viscoelastic Deformation. Thermal: Heat Capacity, Thermal Expansion, Thermal Conductivity, Thermal Shock, Failure Analysis and Prevention (6)

SECTION-B

Phase Diagrams: The Phase Rule, the Phase Diagram, the Lever Rule, Heat Treatment, Time the Third Dimension the TTT Diagram, Hardenability, Precipitation Hardening Annealing, The Kinetics of Phase transformations for Nonmetals. (5)

Structural Materials & Processing: Metals, Ceramics, and Glasses, Polymers and Composites, Processing all four Structural Materials, Electronic Materials**:** Charge Carriers and Conduction, Energy Levels and Energy Bands, Conductors, Insulators, Semiconductors, Composites, Electrical Classification of Materials (6)

Optical and Magnetic Materials: Optical Materials, Magnetic Materials, Materials in Engineering Design, Selection of Electronic, Optical, and Magnetic Materials (4)

Advanced Semiconductor Materials: Band structure, carrier concentration, Electrical Mechanical and optical properties of Gallium Nitride, Aluminium Nitride, Indium Nitride, Boron Nitride, Silicon Carbide, Silicon-germanium (Sil-xGex), Materials of special applications viz. cryogenic, high temperature, high frequency Applications. (6)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Properties of Advanced Semiconductor Materials: Gan, Aln, Inn	Michael E .Levinshtein	Springer. 2001
RECOMMENDED BOOKS			
1	Introduction to Materials Science for Engineers, 6th Edition	James F. Shackelford	Prentice Hall.2001
2	Fundamentals of Semiconductors: Physics and Materials properties	Yu and M Cardona	Springer, 1996

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-107**
Course Title	**EMBEDDED SYSTEM DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Introduction: A system, processors and other hardware units for embedded systems, Embedded into system, microprocessor, microcontroller, single processor; regular processors and microcontrollers for embedded systems. Examples of Embedded System. (4)

Hardware Aspects: Embedded microcontroller cores, Brief discussion about processor structure: GPP, ASISP, System Processor, Application specific system processor; registers; memories: RAM, ROM, UVROM, EEPROM, Flash Memory, DRAM; parallel and serial communication and ports; timers and interrupts. (8)

Programming Tools and handheld Devices: Using embedded C++, use of RTOS μc/os-I I, use of RTOS VxWorks, Kernel of an embedded system and device drivers. (12)

SECTION-B

Using Multiple Processors in Embedded Systems: Multiple process in parallel, modelling tools for a multiprocessor system, distributed embedded systems, Systems on chip(SOC). (8)

Design of an embedded system: System design, design cycle development phase for an embedded system, users of target systems, emulator and ICE, use of software tools for embedded systems, scopes and analyzers for system hardware test; Technological aspects of embedded systems: interfacing between analog and digital blocks, signal conditioning, digital signal processing. (13)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Embedded Systems	Raj Kamal	Tata Mcgraw Hill. 2004
RECOMMENDED BOOKS			
1	Embedded System Design	Frank Vahid & Tony Givargis	John Wily & Sons.1998
2	Embedded System Design – An Introduction to Processes, Tools & Techniques	Arnold S. Berger	CMP Books.2000
3	Real Time Systems	W.S. Liu Jane	Pearson Education.2003
4	Specification and Design Methodology for Real Time Embedded Systems	Janka S. Randall	CMP Books.2000
5	The Art of Designing Embedded Systems	Jack Ganssle	Newnes, 1999
6	Embedded Microcomputer System: Real Time Interfacing	J.W. Valvano	Brooks/Cole, 2000

PRACTICALS:

Practical based on theory will be conducted

SECOND SEMESTER

Course Code	**MIC-201**
Course Title	**DIGITAL INTEGRATED CIRCUITS & SYSTEMS**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Introduction: Digital Systems; Data representation and coding; Levels of Abstraction, Logic circuits, integrated circuits; Analysis, design and implementation of digital systems. (4)

Combinatorial Logic Systems: Definition and specification; Truth table; Basic logic operation and logic gates. Boolean Algebra and Switching Functions**:** Basic postulates and fundamental theorems of Boolean algebra; Standard representation of logic functions - SOP and POS forms; Simplification of switching functions - K-map and Quine-McCluskey tabular methods; Synthesis of combinational logic circuits, encoders, Parity circuits and comparators; Arithmetic modules-adders, subtractors and ALU. (10)

Logic families: Operational characteristics of MOSFET as switch; CMOS inverter - circuit description and operation; Structure and operations of CMOS gates; Electrical characteristics of logic gates – logic levels and noise margins, fan-out, propagation delay, transition time, power consumption and power-delay product. (10)

SECTION-B

Sequential Logic systems: State machines, state machine as a sequential controller; Basic sequential circuits- latches and flip-flops: SR-latch, D-latch, D flip-flop, JK flip-flop, T flip-flop; Timing hazards and races; Analysis of state machines using D flip-flops and JK flip-flops; Design of state machines - state table, state assignment, transition/excitation table, excitation maps and equations, logic realization; Design examples (9)

State Machine Design Approach: Designing state machine using ASM charts; Designing state machine using state diagram. (4)

Sequential Logic Modules and Applications: Multi-bit latches and registers, counters, shift register, application examples-.High speed adders, multipliers, FIFOs, and Barrel shifters, ALU control semiconductors for memories and PLAs, microprogrammed and PLA based control design. Programmable Logic Devices: PLAs, PALs and their applications; Sequential PLDs and their applications; State machine design with sequential PLDs; Introduction to field programmable gate arrays (FPGAs) (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Digital Design: Principle and practices	John F. Wakherly	PHI International, 1994
2.	Principles of Digital Design	Daniel D.Gajski	Prentice Hall
RECOMMENDED BOOKS			
1	Digital Circuits: A proportion for Microprocessors	Charles Mckay	Prentice Hall
2	Fundamentals of Digital Circuits	A. Anand Kumar	PHI

PRACTICALS:

Practical based on theory will be conducted

Course code	**MIC-202**
Course Title	**MEASUREMENT AND CHARACTERIZATION TECHNIQUES**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Introduction to materials and techniques, Structure analysis tools: X-ray diffraction; Reflection High energy electron Diffraction (RHEED), Low energy Electron Diffraction (LEED), Transmission Electron Microscopy (TEM); (8)

Basic Electron scattering, Concepts of resolution, TEM instruments, Various imaging modes, Analysis of micrographs, Electron Energy Loss Spectroscopy; Scanning Electron Microscopy, Rutherford backscattering spectrometry; Atomic Force Microscopy, Scanning Probe Microscopy. (8)

Electrical Characterization Techniques: Electrical resistivity in bulk and thin films, Hall effect, Magnetoresistance; (7)

SECTION-B

Optical Characterization Techniques: UV-VIS spectroscopy, Fourier transform infrared spectroscopy, Raman spectroscopy, X-ray photoelectron spectroscopy. (8)

Electron Beam Techniques: Electron Beam Induced Current (EBIC) and voltage contrast technique. (6)

Auger Electron Spectroscopy(AES), Electron Microphone (EDX), LEED, RHEED, Ion beam Techniques (SIMS, RBS), X-ray techniques (XPS, X-ray Topography). (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Semiconductor Measurement and Instrumentation	W.R. Runyan	McGraw Hill
2.	Solid State Electronic Devices	Ben G. Streetman	Pearson,2015
RECOMMENDED BOOKS			
1	Imperfections and Impurities in Semiconductor Silicon	K.V. Ravi	John Wiley and Sons
2	Characterization of Semiconductor Materials	Philip F. Kare and Greydon B. Laubee	Mc-Graw Hill

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-203**
Course Title	**ARCHITECTURE OF VLSI SYSTEMS**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

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SECTION-A

Overview of architectural schemes, organization, systems representation: structural, behavioural, data flow; Arithmetic and Logical operation and hardware implementation, Software implementation of some complex operation. Introduction to memory Unit, control unit and Instruction Set, Working with an ALU, Concepts of Machine level programming, Assembly level programming and High level programming. Various addressing modes and designing of an Instruction set, Concepts of subroutine and subroutine call , Use of stack for handling subroutine call and return (8)

Introduction to CPU design, Instruction interpretation and execution, Micro-operation and their RTL specification, Hardwired control CPU design, Microprogrammed control CPU design. (8)

Concepts of semiconductor memory, CPU- memory interaction, organization of memory modules, Cache memory and related mapping and replacement policies,Virtual memory (7)

SECTION B

Introduction to input/output processing, working with video display unit and keyboard and routine to control them, Programmed controlled I/O transfer, Interrupt controlled I/O transfer, DMA controller, Secondary storage and type of storage devices, Introduction to buses and connecting I/O devices to CPU and memory. (8)

CISC Vs RISC, Introduction to pipelining and pipeline hazards, design issues of pipeline architecture, Instruction level parallelism and advanced issues., Introduction to interconnection network and practical issues, Examples of interconnection networks. Multiprocessors and its characteristics, Memory organization for multiprocessors systems (8)

synchronization and models of memory consistency, Issues of deadlock and scheduling in multiprocessor systems, Cache in multiprocessor systems and related problems, Parallel processing concepts, Parallelism algorithm for multiprocessor systems. (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Computer Architecture and Organization	J.P Hayes	Mc.Graw Hill. 1998
RECOMMENDED BOOKS			
1	Computer Architecture	Nicholas Carter, Schaum's outlines	McGraw Hill.2001
2	Computer system organization and Architecture	Carpinellie	Pearson Education. 2001
3	Parallelled Algorithms for VLSI Computer Aided Design	Prithviraj Banerjee	PTR Prentice Hall. 1992

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-204**
Course Title	**ANALOG AND MIXED SIGNAL DEVICE DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION-A

Basic MOS Device physics: Analog VLSI issues in CMOS technologies, Basic MOS Models, SPICE Models and frequency dependent parameters, Basic NMOS/CMOS Gain stage. (8)

Single stage amplifiers: basic concepts, common-source stage, source follower, common-gate stage, Current sources and sinks. (6)

Passive and Active Current Mirrors: basic current mirrors, cascode current mirrors, active current mirrors, Voltage and current references. (6)

SECTION-B

Differential Amplifier: Single ended and differential operation ,basic differential pair ,common mode response ,differential pair with MOS loads ,Gilbert Cell. (8)

Operational Amplifiers:Basic design parameters of op-amp design. Compensation of op-amp. Basics design concept of 741 op-amp design. MOS Differential amplifier. (8)

CMOS op-amps: Design of CMOS op-amp, design of one stage op-amp. (6)

Analog-to-Digital Converters: serial A/D converters,Successive approximation A/D converters, Analog Multipliers (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	CMOS Analog Circuit Design, second edition	Philip E.Allen,Douglas R.Holberg	Newyork: Oxford 2006
RECOMMENDED BOOKS			
1	Design of Analog CMOS Integrated Circuits	B. Razavi	McGraw- Hill, 2001.

PRACTICAL

- Simulation of analog integrated circuits
- Simulation & characterization of mixed signal devices

Course Code	**MIC-205**
Course Title	**ADVANCED MEMORY TECHNOLOGY AND DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION A

INTRODUCTION TO MEMORY CHIP DESIGN: Internal Organization of Memory Chips, Memory cell Array, Peripheral Circuit, I/O Interface categories of Memory Chip, Basic Operation of 1-T Cell, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology. (8)

BASICS OF RAM DESIGN AND TECHNOLOGY: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law. (8)

ON-CHIP VOLTAGE GENERATORS: Substrate-Bias Voltage(VBB) Generator, Voltage Up-converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-chip Voltage Generators. (8)

SECTION B

DRAM CIRCUITS: High-Density Technology, High-Performance Circuits, Catalog Specification of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data line and Word line, Read and Relevant Circuits, Write and relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-chip testing Circuits, High Signal-to-Noise ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources. (11)

HIGH-PERFORMANCE SUBSYSTEM MEMORIES: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. (10)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Semiconductor Memories: Technology, Testing, and Reliability	Ashok K. Sharma	Wiley-IEEE Press,2002
RECOMMENDED BOOKS			
1	Advanced Semiconductor Memories: Architectures, Designs, and Applications	Ashok K. Sharma	Wiley-IEEE Press,2002
2	Semiconductor Memories: A handbook of Design, Manufacture and Application,	Betty Prince	Wiley- IEEE Press, *2nd Edition*
3	Ferroelectric Memories	James Scot	Springer publications
4	Flash memories	Paolo Cappelletti, Carla Golla, Piero Olivo, Enrico Zanoni, Kluwer	Academic Publishers, Boston
5	Emerging memories, Technologies and Trends	Betty Prince	Kluwer Academic Publishers.

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-206**
Course Title	**MEMS AND MICROSYSTEMS**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION A

Overview, Working principle of microsensors & microactuation (4)

Scaling of Forces : 1.1 Scaling of Forces Model, Weight, Example: MEMS Accelerometer, Elastic Force, Example: AFM Cantilever, Electrostatic Force, Example: MEMS RF Switch, Piezoelectric Force. Elasticity : Stress, Strain, Stress–strain Relationship, Example: Plane Stress, Strain–stress Relationship in Anisotropic Materials, Miller Indices, Example: Miller Indices of Typical Planes. (8)

Bending of Microstructures: Static Equilibrium, Free Body Diagram, Neutral Plane and Curvature, Pure Bending, Neutral Plane for a Rectangular Cross-section, Example: Cantilever with Point Force at the Tip, Moment of Inertia and Bending Moment, Example: Moment of Inertia of a Rectangular Cross-section, Beam Equation, End-loaded Cantilever, Equivalent Stiffness, Beam Equation for Point Load and Distributed Load. (10)

SECTION B

Piezoresistance: Electrical Resistance, Example: Resistance Value, One-dimensional Piezoresistance Model, Example: Gauge Factors, Piezoresistance in Anisotropic Materials, Two-dimensional Piezoresistors, Example: Accelerometer with Cantilever and Piezoresistive Sensing, Pressure Sensing with Rectangular Membranes. (8)

Electrostatic Driving and Sensing: Energy and Co-energy, Voltage Drive, Pull-in Voltage, Forces in a Parallel-plate Actuator, Electrostatic Pressure, Contact Resistance in Parallel-plate Switches, Capacitive Accelerometer. (8)

Fabrication: Introduction, Photolithography, Patterning, Lift-off, Bulk Micromachining, Angle of Walls in Silicon (100) Etching, Surface Micromachining, Example: Cantilever Fabrication by Surface Micromachining. (7)

TEXT BOOK			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Understanding MEMS: Principles and Applications	Luis Castaner	Wiley Publication, 2015
REFERENCE BOOK			
1	MEMS & Microsystem- Design & Manufacture	Tai-Ran Hsu	Tata McGraw Hill.2002

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-207**
Course Title	**RF AND HIGH SPEED DIGITAL DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt any two questions from each part.*

SECTION-A

Introduction to RF and wireless : Complexity comparison, Design bottle necks, Applications, Analog and digital systems, Choice of Technology. Basic Concepts In RF Design: Nonlinearity and time variance, ISI, Random process and noise, sensitivity and dynamic range, conversion gains and distortion, passive impedance transformation. Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. (12)

Multiple Access: Techniques and wireless standards, mobile RF communication, FDMA, TDMA, CDMA, Wireless standards. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation. (12)

SECTION B

Transceiver Architecture : General considerations, receiver architecture, Transmitter Architecture, transceiver performance tests, case studies. Amplifiers, Mixers and oscillators LNAs, down conversion mixers, Cascaded Stages, oscillators, Frequency synthesizers. (8)

Power Amplifiers: General considerations, linear and nonlinear Pas, classification, High Frequency power amplifier, large signal impedance matching, linearization techniques. (6)

High speed Design: Ideal transmission line fundamentals, Crosstalk, Non Ideal interconnect issues, connectors packages and vias, Non ideal return paths, simultaneous switching noise, and power delivery, buffer modeling, digital timing analysis, timing specific design methodologies, radiated emissions compliance and system noise minimization, high speed measurement techniques. (8)

TEXT BOOK			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	High- Speed Digital System Design	Stephen H.Hall	Springer.2001
REFERENCE BOOK			
2	Practical RF Circuit Design for Modern Wireless Systems, Volume I : Passive Circuits and Systems	Les Besser	Rowan Gilmore

PRACTICALS:

Practical based on theory will be conducted

THIRD SEMESTER

Course Code	**MIC-301**
Course Title	**LOW POWER DIGITAL CMOS DESIGN**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION-A

Hierarchy of Limits of Power: Introduction, Theoretical Limits: fundamental limits, material limits, device limits, circuit limits, system limits. (6)

Sources of power consumption: switching component of power-switching energy per transition, activity factor, influence of logic level statistics on activity factor- type of logic function, type of logic style, signal statistics, inter signal co-relations, short circuit component of power, leakage component of power. (8)

Power Estimation, Synthesis for low power- behavioral level, logic level, circuit level, Voltage scaling approaches. (8)

SECTION-B

Design and test of low power circuits, Adiabatic switching, Minimizing switched capacitance. **Low Energy Computing using Energy Recovery Techniques,** (4)

Low Power SRAM Architecture: organization of static RAM,MOS SRAM memory cell operations-4T, 6T,banked organizations of SRAM, reduced voltage swings on bit line, reduced power in -write driver circuit, sense amplifier circuit (8)

Low power Programmable computation: architectural approaches to low power, shutdown techniques, conventional shutdown approaches- rest mode, sleep mode, shutdown mode, predictive shutdown approaches, architectural voltage driven reduction. (7)

Software design for low power: sources of software power dissipation, power estimations, power optimization. (4)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Low power CMOS VLSI Circuit Design	Kaushik Roy and Sharat Parsad	John Wiley & Sons.1998
RECOMMENDED BOOKS			
1	Low Power Digital CMOS Design	A.P. Chandrakasan and R Brodersen	Kluwer Academic Publishers. 1995
2	Low Power Design Methodoligies	J.M. Rabaey and M. Pedram	KJ Academic Publishers. 2001
3	Designing CMOS Circuits for Low Power	Dimitrios Soudris, Christian Piguet and Costas Goutis	Kluwer Academic Publishers. 2000

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-302**
Course Title	**Microelectronics Packaging and Testing**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION-A

PACKAGING: Introduction, Packaging Hierarchy, Package parameters, packaging substrates, package types, Hermetic packages, die attachment techniques, package parasitic, package modeling, packaging in wireless application, future trends. (11)

BASICS OF TESTING AND FAULT MODELING Introduction- Principle of testing, types of testing -DC and AC parametric tests, fault modeling, Stuck-at fault, fault equivalence, fault collapsing, fault dominance, fault simulation- Event driven simulation, serial simulation, parallel simulation, concurrent simulation. (12)

SECTION-B

TESTING AND TESTABILITY OF COMBINATIONAL CIRCUITS Test generation basics - Automatic test pattern generation, ATPG algorithm, types of ATPG algorithm, D algorithm , PODEM, Testable combinational logic circuit design. (6)

MEMORY, DELAY FAULT AND IDDQ TESTING Testable memory design - RAM fault models - test algorithms for RAMs – Delay faults - Delay test- IDDQ testing - testing methods - limitations of IDDQ Testing, boundary scan test, boundary scan controller. (8)

BUILT-IN SELF-TEST Test pattern generation of Built-in Self-Test (BIST) – LPSR and MISR. (8)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Microelectronics Packaging Handbook: Semiconductor Packaging Part I, II, III	R.R. Tummals et. al.	Kluwer Academic Publishers
RECOMMENDED BOOKS			
1	Circuits, Interconnects & Packaging for VLSI	H.B.Bakoglu	Addison Wesley
2	Fundamentals of Microfabrication	Marc Madou	CRC Press. 1990
3	Digital Systems Testing and Testable design	Miron Abramovici, Melvin A. Breuer & Arthur D. Friedman	Jaico publishing House. 2002
4	VLSI Fault Modeling and Testing Techniques	G.W.Zobrist	Albex Publishers. 1995
5	Testing and Diagnosis of VLSI and ULSI	F. Lombardi and M. Sami	Kluwer Academic Publishers. 1996
6	Neural Models and Algorithms for Digital Testing	S.T. Chakradhar, U.D. Agrawal & M.L Bushnell	Kluwer Academic Publishers. 1996
7	Testing and Reliable Design of CMOS Circuits	N.K. Jha & S. Kurdu	Kluwer Academic Publishers. 1996

PRACTICALS:

Practical based on theory will be conducted

Course Code	**MIC-303**
Course Title	**NANOSCALE DEVICES AND SYSTEMS**
Type of Course	**Core**
L T P	**3 0 2**
Credits	**4**
Course Assessment Methods **End Semester Assessment (University Exam.)** **Continuous Assessment (Sessional, Assignments, Quiz)**	 **50** **50**

SYLLABUS

Note for Examiner- *Examiner will set 7 questions of equal marks. First question will cover whole syllabus, having 10 conceptual questions of 1 mark each or 5 questions of 2 mark each and is compulsory. Rest of the paper will be divided into two parts having three questions each and the candidate is required to attempt at least two questions from each part.*

SECTION A

Nanostructures: Introduction, Progressing technology, macroscopic observables in nanostructures, Ballistic transport, Phase interference, Carrier heating in nanostructures. (10)

Quantum confined systems: Nanostructure materials, Lateral confinement: Quantum wires and quantum dots, Nanolithography, Quantum wire and quantum dot structures,Electronic states in quantum wires and quantum dots,Magnetic field effects in quantum confined systems, Transmission in nanostructures**,** Tunnelling in planar barrier structures**,** Wave function treatment of tunnelling,Current in resonant tunnelling diodes, Singleelectron effects and Coulomb Blockade, Introduction to Nano electro mechanical systems(NEMS). (12)

SECTION B

Introduction to Molecular electronic devices, self-assembled monolayers (SAM), Diodes, Optoelectronic Devices, Switches, Nanowires, programmable logic arrays, digital gates, flip-flops, shift registers, memories, rectifiers, Overview of Nano materials. (12)

Nano Fabrication Techniques: Lithography, Self- Assemble, contact imprinting and Binding of organics and semiconductors. (11)

TEXT BOOKS			
S. No.	NAME	AUTHOR(S)	PUBLISHER
1	Transport in Nanostructures	Ferry, David K. and Goodnick, Stephen Marshall	Cambridge University Press
RECOMMENDED BOOKS			
1	Nanotechnology	G. Timp	Bell Labs, Murray Hill, NJ (Ed.)
2	Molecular electronic devices, Part II	F.L. Carter, Forrest. L	Marcel and Dekker
3	Nano Systems: Molecular machinery, manufacturing and computation	Eric Drexler	John Wiley and sons.
4	Organic electroluminescent materials and devices	S Miyata, H.S.Nalwa. Gordon and breach science	Amsterdam, 1997
5	Organic semiconductors	Felix Gutmann, Lawrence Elyons	John Wiley & Sons

PRACTICALS:

Practical based on theory will be conducted

Preliminary Thesis and Thesis

Each student will be required to work on the Preliminary Thesis and Thesis approved by department faculty that will span III and IV semesters during which periodic progress reports will be monitored. At the end of III semester, Preliminary Thesis progress will be evaluated by the departmental faculty.

At the end of IV semester, the student will submit the Thesis.