[4063] – 278

T.E. (E &TC) (Semester – II) Examination, 2011
COMPUTER ORGANISATION AND ARCHITECTURE
(2008 Pattern) (New)

Time : 3 Hours Max. Marks : 100

SECTION – I

1. a) Explain the operation of sequential circuit binary multiplier with

   Multiplicand 1101

   Multiplier 1011. **8**

   b) Using Booth's algorithm multiply

   Multiplicand = – 13

   Multiplier = + 11 **8**

   OR

2. a) Explain following addressing modes with example
      1) Indirect mode
      2) Index mode
      3) Relative mode. **6**

   b) Carry out bit pair recoding of following multipliers

   1 1 0 1 0

   0 1 1 0 1 **4**

   c) Represent (178.1875) in single precision floating point format. **6**

3. a) Explain with neat block diagram single bus organisation. **9**

   b) Using input output gating for the registers in single bus organisation explain operation of
      1) Fetching a word from memory
      2) Storing a word in memory. **9**

   OR

P.T.O.

4. a) Draw neat block diagram of three bus organisation of data path inside the processor and hence explain the control sequence for instruction Add R4, R5, R6. **9**

   b) What is microprogrammed control ? Using single bus organisation write control sequence for execution of instruction Add (R3), R1. Write microinstructions for the same. **9**

5. a) Explain how multiple interrupt requests can be handled using
      1) Vectored Interrupt
      2) Using individual interrupt request and acknowledge lines. **6**

   b) Explain use of PCI bus in computer system. Also explain data transfer signals on PCI bus. **10**

OR

6. a) Write notes on :
      1) USB
      2) Cache Memory. **16**

SECTION – II

7. a) Explain 8086 architecture. **8**

   b) With suitable example explain difference between rotate and shift instructions. **4**

   c) Explain with suitable example how physical address of operand is calculated in 8086. **4**

OR

8. a) Explain interrupt vector table of 8086. **8**

   b) Explain string instructions of 8086. **8**

9. a) Explain flag register of 80386. **8**

   b) Explain memory paging mechanism in 80386. **8**

OR

10. a) Explain segment descriptor in detail. **8**

    b) Explain the use of various registers in 80386. **8**

11. a) What is the difference between loosely coupled and tightly coupled multiprocessor system ? **6**

    b) Compare RISC and CISC. **6**

    c) Explain pipelining mechanism of RISC processor. **6**

OR

12. a) List and explain various registers in ARM core. What are different modes of operation in ARM ? **5**

    b) Explain superscalar processor architectures. **8**

    c) Explain role of Barrel shifter in ARM core data flow model. **5**

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