Code No: X0524/R07 **Set No. 1**

II B.Tech I Semester Supplementary Examinations, Apr/May 2012
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering and Information Technology)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Generate Hamming code for the given 11 bit message 11001001100 and rewrite the entire message with Hamming code.
   (b) The binary numbers listed have a sign bit in the left most position and , if negative numbers are in 1's complement form. Perform the arithmetic operations indicated and verify the answers. [8+8]
   i. 101011 + 111001
   ii. 001111 + 110010
   iii. 111001 - 011010
   iv. 101111 - 100110.

2. (a) Reduce the following Boolean expressions.
   i. AB' (C + BD) + A'B'
   ii. A'B'C + (A + B + C')' + A'B'C'D
   iii. ABCD + AB(CD)' + (AB)'CD
   iv. (A + A')(AB + ABC').
   (b) Obtain the complement of the following Boolean expressions. [8+8]
   i. ABC + A'B + ABC'
   ii. (BC' + A'D)(AB' + CD')
   iii. x'yz + xz
   iv. xy + x (wz + wz').

3. (a) Implement the following Boolean expression with Excusive-NOR and NOR gates:
   $F = A\overline{B}C\overline{D} + \overline{A}BC\overline{D} + A\overline{B}\ \ \overline{C}D + \overline{A}B\overline{C}D$
   (b) If $F_1 = wx\overline{y}+\overline{y}\ \ \overline{z}+\overline{w}y\overline{z}+xy\overline{z}$ And $F_2 = (w + x + \overline{y} + \overline{z})\,(\overline{x} + \overline{y} + z)\,(\overline{w} + y + \overline{z})$ Obtain minterms list of $F_1 \bullet F_2$ using K-map obtain minimal SOP function of $F_1 \bullet F_2$. [8+8]

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

Code No: X0524/R07 **Set No. 1**

5. A circuit is to be designed with two inputs (X, Y) and one output 'Z'. The logic is Z = X if Y = 1, but if Y = 0, 'Z' is remain fixed at its last value before 'Y' becomes zero. Derive state diagram and state table and design the circuit using D-flip-flops. [16]

6. Draw the logic diagram for 4-bit up down binary counter using T- flip flops and explain the operation with state table and state equations. [16]

7. (a) Give the HDL code for a memory read, write operations if the memory size is 64 words of 4 bits each. Also explain the code.

   (b) A 16K * 4 memory uses coincident decoding by splitting the internal decoder into X-selection and Y-selection. [8+8]

      i. What is the size of each decoder and how many AND gates are required for decoding the address?

      ii. Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000.

8. (a) Give the implementation procedure for a SR Latch using NOR gates.

   (b) An asynchronous sequential circuit is described by the excitation and output functions.
   $Y = x_1x_2' + (x_1 + x_2')y$
   $Z = y$
   Implement the circuit defined above with a NOR SR latch. Repeat with a NAND SR latch. [6+10]

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1. A 12-bit Hamming code word containing 8-bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written in to memory if 12-bit words read out is as follows? [4×4]
   (a) 000011101010
   (b) 101110000110
   (c) 101111110100
   (d) 110011010010.

2. (a) Express the following functions in sum of minterms and product of maxterms.
      i. F (A,B,C,D) = B'D + A'D + BD
      ii. F(x,y,z) = (xy + z)(xz + y).
   (b) Obtain the complement of the following Boolean expressions. [8+8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C').

3. (a) Implement the following function in NAND-NAND and NOR - NOR two level forms and draw the circuits.
      $f(A, B, C, D) = \prod 5, 6, 7, 10, 11, 13, 14, 15$
   (b) Implement two input exclusive - NOR circuit using multilevel NAND form and draw the circuit. [10+6]

4. (a) If $F_1(A, B, C, D) = \Sigma(1, 3, 4, 5, 9, 10, 11) + d(6, 8)$ and
      $F_2(A, B, C, D) = \Pi(1, 3, 5, 6, 10, 11, 13, 14) + d(9, 12)$
      Design a minimal SOP logical circuit for $F_3(A, B, C, D) = F_1 \oplus F_2$
      Draw the circuit using NOR- gates.
   (b) Design a Code converter circuit to convert 9's complement code to BCD code using Full-adders and additional gates. (Use block diagram of Full adders). [8+8]

5. (a) Explain the operation of D-flip-flop with negative edge triggering using NAND gates.

Code No: X0524/R07 **Set No. 2**

(b) Obtain the state diagram for the synchronous sequential circuit with two inputs (X, Y) and one output 'Z'. The input represents alphabet letters as 00 -A, 01-B, 10-C and 11-D. The output is one if the most recent two inputs are in alphabetic order, i.e., AB, BC, CD. [6+10]

6. (a) Draw the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops.

   (b) Write the HDL behavioral description of the 4- bit universal shift register. [8+8]

7. (a) Show the memory cycle timing waveforms for the write and read operations. Assume a CPU clock of 50 MHz and a memory cycle time of 50 ns.

   (b) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? [8+8]

   i. 4K * 16,
   ii. 2G * 8 ,
   iii. 16M * 32,
   iv. 256K * 64.

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.

   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are:
   Y1 = $x_1x_2 + x_1y_2' + x_2'y_1$
   Y2 = $x_2 + x_1y_1'y_2 + x_1'y_1$
   z= $x_2 + y_1$ Implement the circuit defined above with NAND SR latches. [8+8]

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1. (a) Express the Decimal Digits 0 - 9 in BCD, 2421, 84-2-1 and Excess-3.
   (b) Convert the Hexadecimal number 1010 to Decimal and then to Binary. [12+4]

2. (a) Find the complement of the following and show that F.F' = 0 and F + F' = 1.
      i. F = xy' + x'y
      ii. F = (x + y' + z)(x' + z')(x + y).
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. B'C'D + (B + C + D)' + B'C'D'E
      ii. AB + (AC)' + (AB + C)
      iii. A'B'C' + A'BC' + AB'C' + ABC'
      iv. AB + (AC)' + AB'C.

3. (a) Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.
   $f(A,B,C,D) = (A+C+D)\left(A+B+\overline{D}\right)\left(A+B+\overline{C}\right)\left(\overline{A}+B+\overline{D}\right)\left(\overline{A}+B+\overline{D}\right)$
   (b) Implement the following Boolean function F using the two - level form: [8+8]
      i. NAND-AND
      ii. AND-NOR $F(A,B,C,D) = \Sigma 0,1,2,3,4,8,9,12$

4. (a) Specify the truth table of an Octal-to-Binary priority encoder. The input with the highest subscript number has the highest priority. What will be the value of the four outputs if inputs D_5 and D_3 are 1 at the same time.
   Assume D_0 through D_7 are octal inputs and x,y,z are the binary outputs.
   (b) With the truth table draw the logic diagram of 3 to 8 line decoder using NOR-gates only. Include an enable input. [8+8]

5. (a) Explain the following terms related to filp-flops.
      i. race round conditions
      ii. propagation delay
      iii. clock.
   (b) Explain the operation of R-S flip-flop with negative edge triggering with neat sketch. And explain its truth table. [8+8]

Code No: X0524/R07 **Set No. 3**

6. (a) Explain synchronous and ripple counters. Compare their merits and demerits.
   (b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. [8+8]

7. (a) What is parity checking? Explain its necessity and how is it implemented?
   (b) How many parity check bits must be included with the data word to achieve single error-connection and double-error detection when the data contains
      i. 16 bits
      ii. 32 bits
      iii. 48 bits. [8+8]

8. (a) Explain critical and non critical races with the help of examples.
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are: [6+10]

$$Y1 = x_1x_2 + x_1y_2' + x_2'y_1$$
$$Y2 = x_2 + x_1y_1'y_2 + x_1'y_1$$
$$Z = x_2 + y_1$$

      i. Draw the logic diagram of the circuit.
      ii. Derive the transition table and output map.
      iii. Obtain a flow table for the circuit.

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1. (a) List the first 20 numbers in base14. Use the letters A, B, C and D to represent the last four digits. [4]
   (b) Convert the following numbers with the given radix to decimal. [4×3]
      i. 4223_5
      ii. 6688_9
      iii. 5654_7
      iv. 667_8.

2. (a) Reduce the following Boolean expressions.
      i. ((AB)' + A' + AB)'
      ii. AB + (AC)' + AB' + C(AB + C)
      iii. ((AB' + ABC)' + A(B + AB'))'
      iv. AB + A(B + C) + B(B + C).
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. x'y' + xy + x'y
      ii. xy' + y'z' + x'z'
      iii. x' + xy + xz' + xy'z'
      iv. (x + y)(x + y').

3. (a) If F_1= Π 3,4,7,8,11,14,15 and F_2= Σ1,2,4,5,7,8,10,11,12,15 obtain minimal SOP expression for $\overline{F_1 \bullet F_2}$ and draw the circuit using NAND gates.
   (b) Draw the two -level NAND circuit for the following Boolean - expression: $\left(A\overline{B} + C\overline{D}\right) E + BC\,(A + B)$ also obtain minimal SOP expression and draw the circuit using NAND gates. [8+8]

4. (a) A multiple output combinational logic circuit is defined by the following functions. Draw the schematic circuits for F_1 and F_2.
   $F_1\,(A, B, C, D) = \overline{\overline{A} \bullet \overline{\overline{A}D}} \bullet \left(\overline{A} + BC\right)$
   $F_2\,(A, B, C, D) = \overline{\overline{A}D} \bullet \left(\overline{A} + BC\right)$
   Using K-Maps simplify F_1 and F_2 and draw the reduced diagram circuit.
   (b) Design a full - subtractor circuit with three inputs x,y,z and outputs D, B. The circuit subtracts X - Y - Z where Z is the input borrow, B is the output borrow and D is the difference draw the circuit using NAND gates. [8+8]

Code No: X0524/R07 **Set No. 4**

5. (a) Draw the circuit diagram for J-K-flip flop using S-R-flip flop with AND gates. Explain its operation using truth table.
   (b) Give the transition table for the following flip-flops. [8+8]
      i. R-S flip-flop
      ii. J-K flip-flop
      iii. T flip-flop
      iv. D flip-flop.

6. Draw the sequential circuit for serial adder using shift registers, full adder and D-FF. Explain its operation with state equations and state table . [16]

7. (a) Explain the construction of a basic memory cell and also explain with diagram the construction of a 4 * 4 RAM
   (b) Given a 32*8 ROM chip with an enable input, show the external connections necessary to construct a 128 * 8 ROM with four chips and a decoder. [8+8]

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.
   (b) An asynchronous sequential circuit has two internal states and one output. The excitation and output functions describing the functions are:
   Y1 = $x_1x_2 + x_1y_2' + x_2'y_1$
   Y2 = $x_2 + x_1y_1'y_2 + x_1'y_1$
   z= $x_2 + y_1$ Implement the circuit defined above with NAND SR latches. [8+8]

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