LAB MANUAL

SUBJECT:

DIGITAL LOGIC DESIGN AND APPLICATIONS

SE (COMPUTERS) SEM III

INDEX

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 1

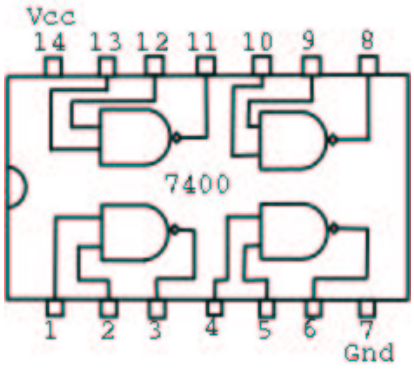
TITLE **STUDY OF BASIC GATES**

AIM To study basic gates.

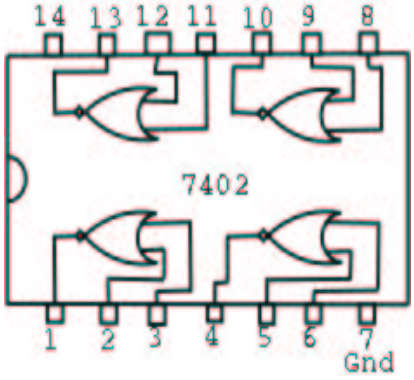
APPARATUS Power Supply, Breadboard, Connecting wires.

COMPONENTS ICs 7400, 7402, 7404, 7408, 7432, 7486, LED.

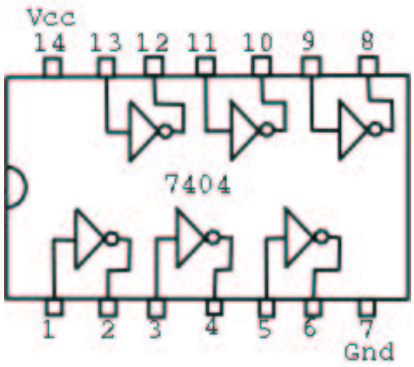
IC PINOUTS **TRUTH-TABLE**



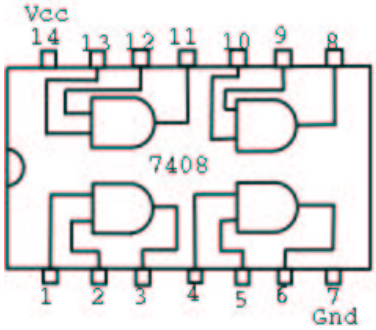
NAND		
A	**B**	**$Y=\overline{A.B}$**
0	0	1
0	1	1
1	0	1
1	1	0



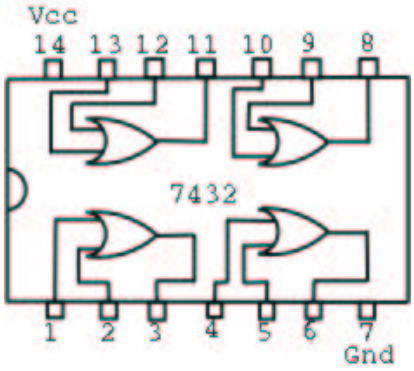
NOR		
A	**B**	**$Y=\overline{A+B}$**
0	0	1
0	1	0
1	0	0
1	1	0



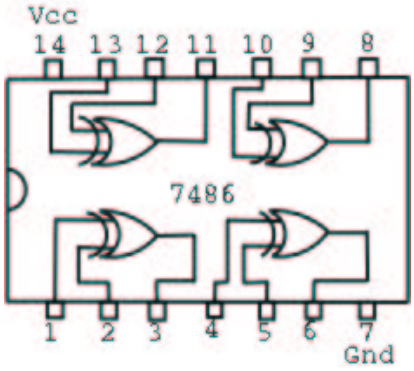
NOT	
A	**$Y=\overline{A}$**
0	1
1	0



AND		
A	**B**	**Y=A.B**
0	0	0
0	1	0
1	0	0
1	1	1



OR		
A	**B**	**Y=A+B**
0	0	0
0	1	1
1	0	1
1	1	1



EX-OR		
A	**B**	**$Y=A\bar{B}+\bar{A}B$**
0	0	0
0	1	1
1	0	1
1	1	1

DIGITAL LOGIC DESIGN AND APPLICATIONS

THEORY

Logic gates are the digital circuits with one output and one or more inputs. They are the basic building blocks of any logic ckt. Different logic gates are : **AND, OR, NOT, NAND, NOR, EX-OR.** They work according to certain logic.

AND : Logic eqn. Y = A.B

The output of AND gate is true when the inputs A and B are True.

OR : Logic eqn. Y = A+B.

The output of OR gate is true when one of the inputs A and B or both the inputs are true.

NOT : Logic eqn. Y = $\bar{A}$.

The output of NOT gate is complement of the input.

NAND : Logic eqn. Y = $\overline{A.B}$

The output of NAND gate is true when one of the inputs or both the inputs are low level. ___

NOR : Logical eqn. Y = $\overline{A+B}$.

The output of NOR gate is true when both the inputs are low.

EX-OR: Logic eqn. Y=$A\overline{B}+\overline{A}B$.

The output of EX-OR gate is true when both the inputs are low.

PROCEDURE

1)Give biasing to the IC and do necessary connections.

2) Give various combinations of inputs and note down the output with help of LED for all gate ICs one by one.

CONCLUSION

Thus all basic gates are studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 2

TITLE **UNIVERSAL GATES**

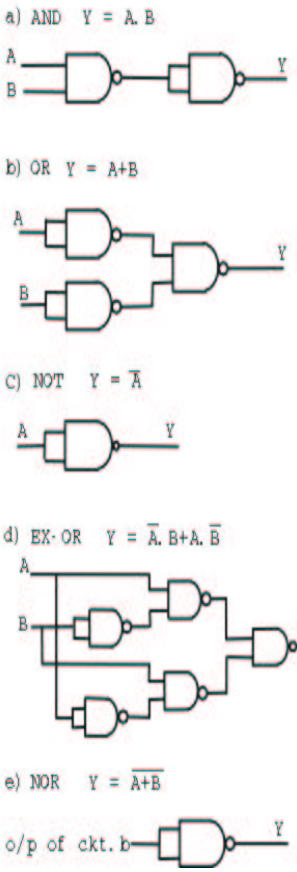
AIM To study the realization of basic gates using universal gates.

APPARATUS Power supply, Breadboard.

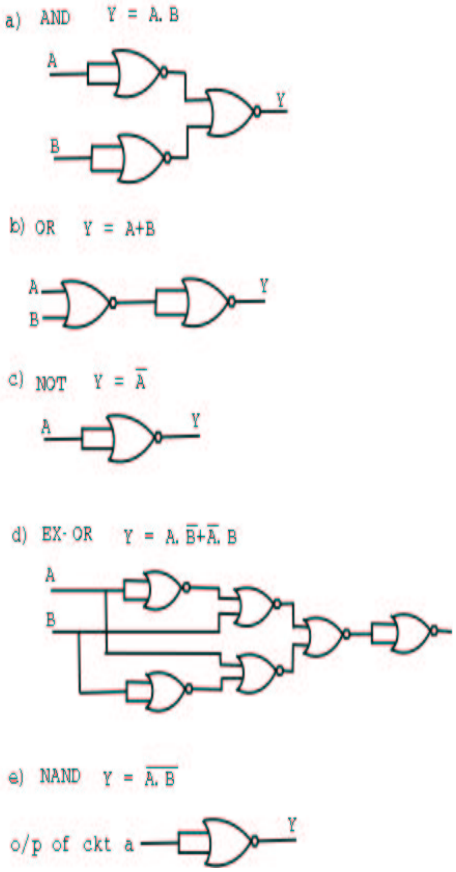
COMPONENTS ICs 7400, 7402, LED.

CIRCUIT DIAGRAM

Using **NAND**



Using **NOR**



DIGITAL LOGIC DESIGN AND APPLICATIONS

THEORY

AND, OR, NOT are called basic gates as their logical operation cannot be simplified further.

NAND and NOR are called universal gates as using only NAND or only NOR any logic function can be implemented. Using NAND and NOR gates and **De Morgans Theorems** different basic gates & EX-OR gates are realized.

PROCEDURE

1)Give biasing to the IC and do necessary connections as shown in the ckt. diagram.

2)Give various combinations of inputs and notedown output using LED.

3) Repeat the procedure for all gates.

OBSERVATION TABLE

A	B	Y
0	0	
0	1	
1	0	
1	1	

CONCLUSION Thus universal gates are studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 3

TITLE **ADDER AND SUBTRACTOR**

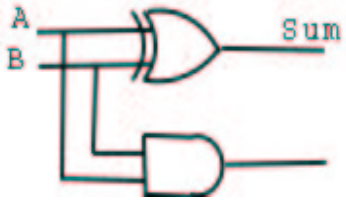
AIM To study adder and subtractor circuits using logic gates.

APPARATUS Power supply, breadboard.

COMPONENTS ICs 7486, 7432, 7408, 7404, LEDs.

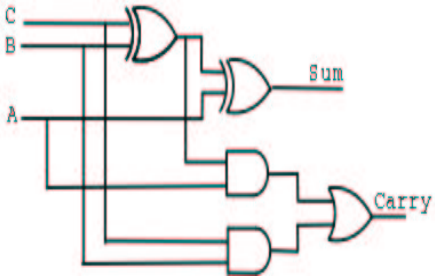
CIRCUIT DIAGRAM AND OBSREVATION TABLE

Half Adder



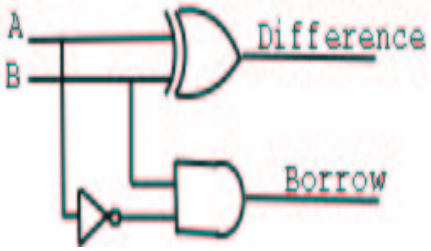
A	B	Sum	Carry
0	0		
0	1		
1	0		
1	1		

Full Adder



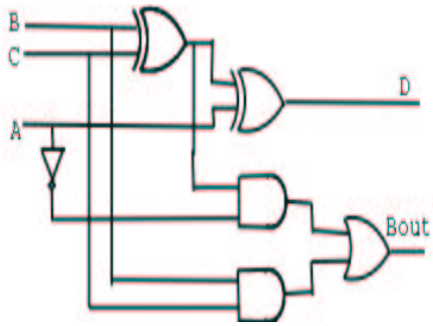
A	B	C	Sum	Carry

Half Subtractor



A	B	Diff.	Bout

Full Subtractor



A	B	C	D	Bout

THEORY A digital adder circuit adds binary signals & a subtractor subtracts binary signals. Half Adder/Subtractor is a basic ckt. that adds / subtracts 2 bits and generates sum or difference along with Carry / Borrow. Unlike half adder or subtractor a full adder / subtractor has the provision to take consideration of previous carry / borrow also.

PROCEDURE A digital adder circuit adds binary signals & a subtractor subtracts binary signals. Half Adder / subtractor is a basic ckt. that adds / subtracts 2 bits and generates sum or difference along with Carry / Borrow. Unlike half adder or subtractor a full adder / subtractor has the provision to take consideration of previous carry / borrow also.

CONCLUSION Thus half & full Adder / Subtractor is studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 4

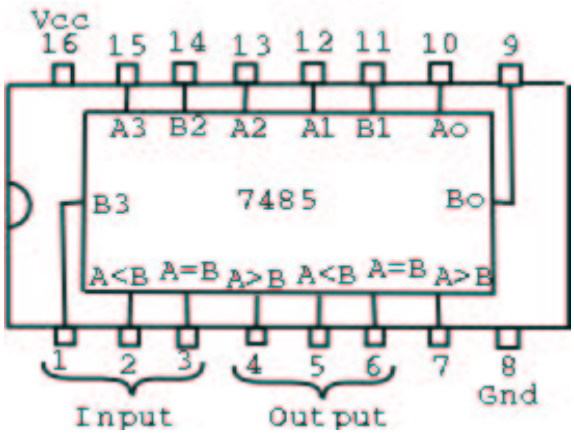
TITLE **MAGNITUDE COMPARATOR**

AIM To study magnitude comparator.

APPARATUS Power supply, Breadboard.

COMPONENTS IC 7485, LEDs.

IC PINOUT



THEORY Magnitude Comparator compares two binary data signals A & B and generates the results of comparision in form of three output signals A>B, A=B, A<B. IC 7485 is a 4-bit comparator. The cascade inputs A>B, A=B, A<B can be used to construct a comparator comparing more than 4 bits. The compare outputs depend on both compare i/ps as well as cascade i/ps.

PROCEDURE

1)Give biasing to the IC .
2)Give various two 4-bit inputs and note down output.
3)Do connections for cascading and note down output for various two 8-bit inputs.

OBSERVATION TABLE

For 4-bit Comparator

A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	A>B	A=B	A<B

CONCLUSION Thus magnitude comparator is studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 5

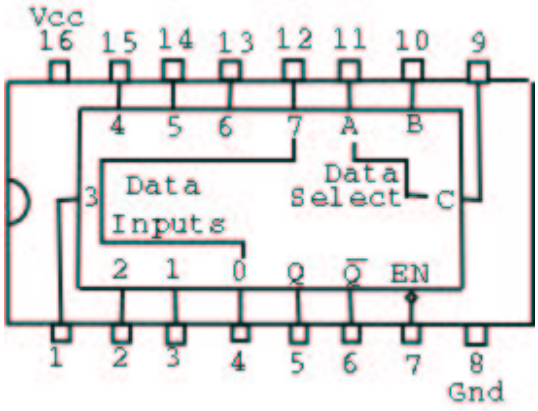
TITLE **MULTIPLEXER**

AIM To study multiplexer.

APPARATUS Power supply, Breadboard.

COMPONENTS IC 74151, LEDs.

IC PINOUT



IC 74151

THEORY Multiplexer is a combinational ckt. that is one of the most widely used in digital design. The multiplexer is a data selector which gates one out of several i/ps to a single o/p. It has n data i/ps & one o/p line & m select lines where $2^m = n$. Depending upon the digital code applied at the select inputs one out of n data input is selected & transmitted to a single o/p channel. Normally strobe(G) input is incorporated which is generally active low which enables the multiplexer when it is LOW. Strobe i/p helps in cascading. A 4:1 Mux. using NAND gate can be designed as shown in dgm 1. No. of ICs are available such as 74157, 74158 (Quad 2:1 mux), 74352, 74153 (dual 4:1 Mux.), 74151A, 74152 (8:1 Mux.), 74150 (16:1 Mux). IC 74151A is a 8 : 1 multiplexer which provides two complementary o/ps Y & $\overline{Y}$. The o/p Y is same as the selected i/$\overline{p}$ & Y is its complement. The n:1 multiplexer can be used to realize a m variable function. ($2^m = n$, m is no. of select inputs)

PROCEDURE 1)Give biasing to the IC.
2)Do necessary connections.

OBSERVATION TABLE

Inputs				Outputs	
Select			Strobe S	Q	$\overline{Q}$
C	B	A			

CONCLUSION Thus multiplexer is studied.

ASSIGNMENT
1)Verify the truthtable of IC 74151, 8:1 Mux.
2)Connect two 74151 ICs in cascading & verify its operation as a 16:1 Mux.
3)Implement the function $Y = A\overline{B}+BC$ using 74151 & verify the truthtable.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 6

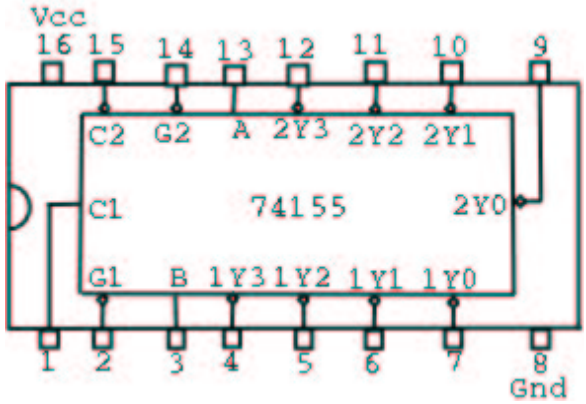
TITLE **DEMULTIPLEXER**

AIM To study demultiplexer.

APPARATUS Power supply, Breadboard.

COMPONENTS IC 74155, LEDs.

IC PINOUT



THEORY Demux takes single i/p & distributes it over several o/ps. It has one data line, n o/p lines & m select lines where $2^m = n$. The logic ckt. of 1:4 demux. using NAND gates is shown in the dgm 1. The ckt. can also be used as binary to decimal decoder with binary inputs applied at the select i/p lines & o/p will be obtained on the corresponding line. MSI ICs available in TTL family for demux. are 74138(3 line to 8 line decoder/demux.), 74139(dual 2 to 4 line decoder/driver.), 74154(4 to 16 line decoder/demux), 74155(dual 2 to 4 line decoder) etc. IC 74155 is a dual 2 to 4 line decoder. It has two sets of active low outputs 1Y0 to 1Y3 & 2Y0 to 2Y3. A & B are the select terminals common for both the demux. C1, C2 & G1, G2 are the data lines & strobe(enable) inputs for the two demux. C1 is active high, C2, G1, G2 are active low. The two 2 line to 4 line demux. can be combined to implement 3 line to 8 line demux.

PROCEDURE 1)Give biasing to the IC.
2)Do necessary connections.

OBSERVATION TABLE **2-Line to 4-Line Decoder OR 1-Line to 4-Line Demultiplexer**

Inputs				Outputs			
Select		Strobe	Data	$1Y_0$ $2Y_0$	$1Y_1$ $2Y_1$	$1Y_2$ $2Y_2$	$1Y_3$ $2Y_3$
B	A	G_1/G_2	C1/C2				

3:8 Decoder OR 1:8 Demultiplexer

Inputs				Outputs							
Select			Strobe (Data)								
C^+	B	A	G‡	$2Y_0$	$2Y_1$	$2Y_2$	$2Y_3$	$1Y_0$	$1Y_1$	$1Y_2$	$1Y_3$

C^+ = I/P's C_1 and C_2 connected together

G‡ = I/P's G_1 and G_2 connected together

CONCLUSION Thus demultiplexer is studied.

ASSIGNMENT 1)Verify the operation of both the demux in IC 74155 as per the truthtable.
2)Combine the two demux to give 3 line to 8 line demux & verify
the operation.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 7

TITLE **FLIP-FLOPS**

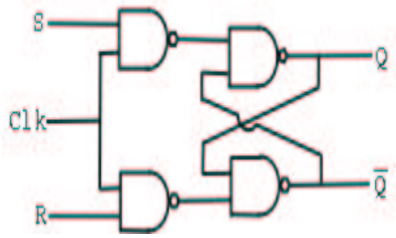
AIM To study R-S, J-K, D and T flip-flops using IC 7476.

APPARATUS Breadboard, Power supply.

COMPONENTS ICs 7400, 7402, 7476, LED.

CIRCUIT DIAGRAM AND TRUTHTABLE

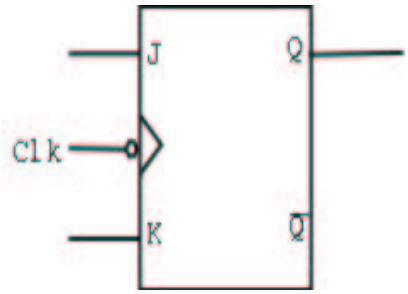
I) SR FF using NAND



Clk	S	R	Qn
0	X	X	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

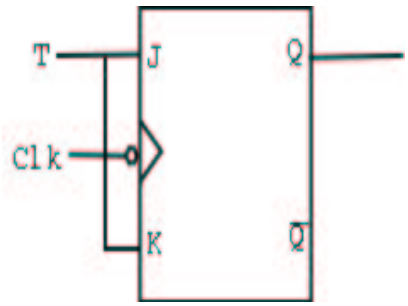
II) JK FF (IC 7476)

1)



Clk	J	K	Qn
↓	0	0	
↓	0	1	
↓	1	0	
↓	1	1	

2) III) T FF using JK



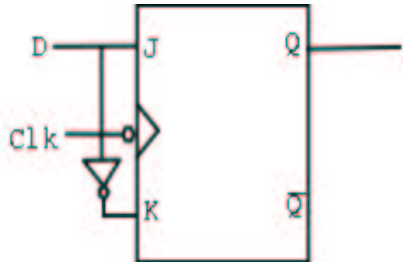
Clk	T	Qn
↓	0	
↓	1	

3)

4)

5) IV) D FF using JK

6)



Clk	D	Qn
⎍	0	
⎍	1	

7)

THEORY Flip-flops are the basic building blocks of sequential ckt. The clocked FFs change their o/p state depending upon i/p's at certain interval of time synchronized with the clock pulse applied to it.
Different types of FFs are S-R, J-K, D & T . Their operations are described by the respective truthtables. MSI chip 7476 incorporates two negative edge triggered Master–Slave JK flipflops. The J-K flipflop can be converted to D & T flipflop.

PROCEDURE 1)Give biasing to the IC and do necessary connections.
2)For various combinations of i/p verify the truthtable.

CONCLUSION Thus R-S, J-K, D & T Flip-Flops are studied.

ASSIGNMENTS 1)Construct clocked S-R FF using only NAND gates & verify the truthtable.
2)Verify the truthtable of J-K FF using IC 7476. Observe the effect of Preset & Clear i/ps.
3)Convert the J-K FF to D & T FF.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 8

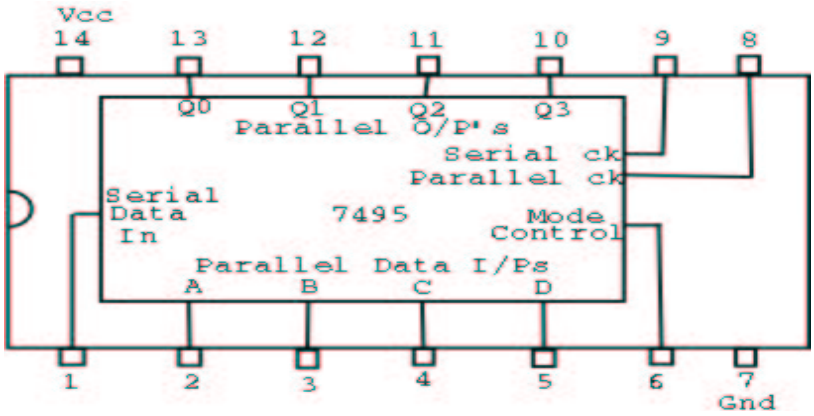
TITLE **SHIFT REGISTER**

AIM To study shift registers.

APPARATUS Power supply, Breadboard.

COMPONENTS IC 7495, LEDs.

IC PINOUT



THEORY A flip-flop stores 1-bit of digital information. It is also referred to as 1-bit register. An array of flip-flops is required to store the no. of bits. This is called register. The data can be entered into or retrieved from the register. So depending on the way how the data can be entered or retrieved there are four possible modes of operation.

1)Serial in serial out (SISO)
2)Serial in parallel out (SIPO)
3)Parallel in serial out (PISO)
4)Parallel in parallel out (PIPO)

Registers can be designed using J-K or S-R as D-type flip-flops and are also available as MSI devices.

The register which can be operated in all possible modes & also the shifting of data is possible in both the directions is called Universal register.

PROCEDURE 1)Give biasing to the IC
2)Do connections for SIPO, PIPO & Left Shift and notedown corresponding o/p.

OBSERVATIONS **I) PIPO : Parallel I/P Parallel O/P**

M	Clk2	A	B	C	D	Q_A	Q_B	Q_C	Q_D
1	0	X	X	X	X				
1									

II) SIPO : Serial I/P Parallel O/P

a) Shift Right

M	Clk1	Serial I / P	Q_A	Q_B	Q_C	Q_D
0						

b) Shift Left

M	Clk2	D I / P	Q_A	Q_B	Q_C	Q_D
1						

CONCLUSION Thus shift register is studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 9

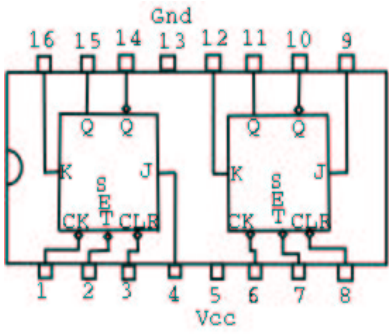
TITLE **COUNTERS**

AIM To study the counters.

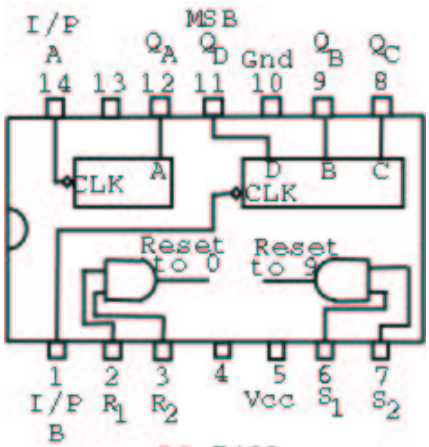
APPARATUS Power supply, Breadboard.

COMPONENTS ICs 7476, 7490, LEDs.

IC PINOUTS

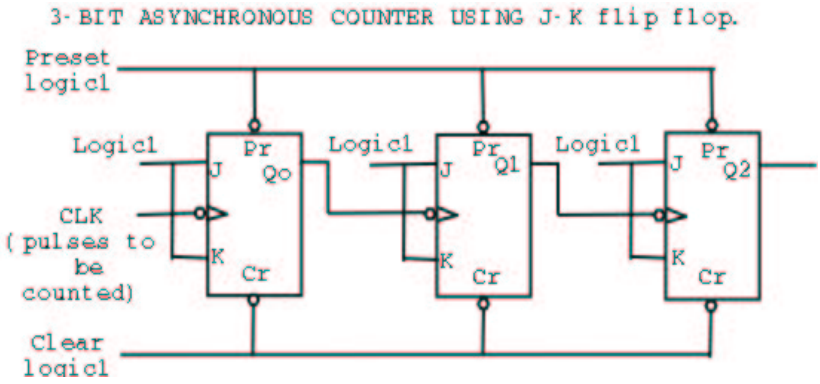


IC7476



IC 7490

CIRCUIT DIAGRAM



DIGITAL LOGIC DESIGN AND APPLICATIONS

THEORY

A ckt. used for counting the pulses is known as counter. Basically there are two types of counters.

1)Asynchronous counter (ripple counter).

2)Synchronous counter.

Asynchronous counter :— In the case of an Asynchronous Counter,all the flip-flops are not clocked simultaneously. This counter is simple in operation & requires a min. of hardware. But its speed is low. Each FF is triggered by a previous FF o/p. Each FF takes its own time to give o/p (due to propagation delay). So final settling time is high. They have the problem of glitch.

Synchronous counter :— In synchronous counters all the Ffs are clocked simultaneously. It is complex in construction, but speed is more. In this case since each FF is clocked simultaneously thus settling time is the delay time of single FF. No problem of glitch.

Asynchronous counter IC (7490) :— It is a BCD counter. It consists of four FFs internally connected to provide a mod-2 counter and a mod-5 counter. The mod-2 and mod-5 counters can be used independently or in combination. FFA operates as a mod2 counter whereas the combination of FFB, FFC and FFD form a mod-5 counter. There are two reset inputs R1 & R2 both of which are to be connected to logic 1 level for clearing all the FFs. The two set inputs S1 & S2 when connected to logic1 level are used for setting the counter to 1001.

PROCEDURE

1)Do connections as per the ckt. dgm.
2)Give biasing to the ICs.
3)Observe o/p using LEDs.

OBSERVATIONS

Counter State	**Q_0**	**Q_1**	**Q_2**
0			
:			
:			
7			

CONCLUSION

Thus counters is studied.

DIGITAL LOGIC DESIGN AND APPLICATIONS

EXPT. NO. 10

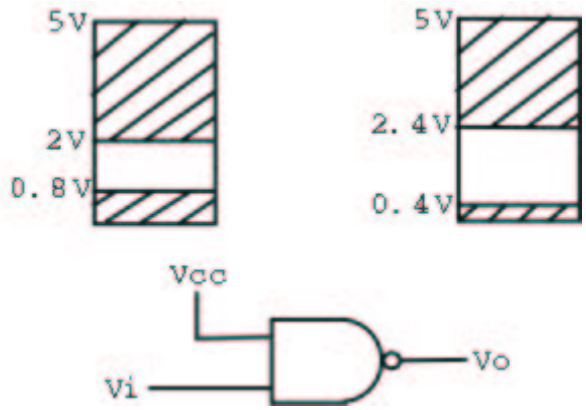
TITLE **TRANSFER CHARACTERISTIC OF TTL AND CMOS**

AIM To study **TTL** & **CMOS** transfer characteristics.

APPARATUS Dual Power supply, Breadboard, Multimeter.

COMPONENTS ICs 74LS00, 74HC00.

CIRCUIT DIAGRAM



THEORY A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific ckt. configuration which is referred to as a logic family. TTL (Transistor-Transistor logic) is one of the saturated Bipolar logic families. CMOS (Complementary metal oxide semiconductor) is an unipolar logic family. Various chars. of digital ICs are used to compare their performances.

Current & Voltage parameters :-

High level i/p voltage V_{IH} :— This is the min. i/p voltage at the o/p corresponding to logic1.

Low level i/p voltage V_{IL} :— This is the max. i/p voltage which is recognized by the gate as logic0.

High level output voltage V_{OH} :— This is the min. voltage available at the o/p corresponding to logic1.

Low level o/p voltage V_{OL} :— This is the max. voltage available at the o/p corresponding to logic0.

PROCEDURE

1)Connect the ckt. as per ckt. dgm. for TTL IC.
2)Vary the i/p voltage in steps & notedown corresponding o/p voltage.
3)Plot graph of Vi Vs Vo.
4)Repeat same procedure for CMOS IC.

OBSERVATIONS

Vi	Vo

CONCLUSION Thus transfer characteristics of **TTL** & **CMOS** ICs is studied.